Current FLIC register maps REVISION 1.5

Last change: 20150806

Hardware Architecture of the FLIC

The FLIC contains four main FPGAs connected to fiber optic serial interfaces and to the ATCA backplane. The FPGAs also are connected to each other by an internal mesh of serial interfaces. Figure 1 shows a photo of a prototype FLIC connected to its rear transition module (RTM). Please note the four large FPGAs in the middle of the board (left-most FPGA has a black heat sink on it the others do not have). The left-most two ***processor*** FPGAs are connected to the silver fiber-optic interface modules at the front of the board (bottom of picture) and also to the fiber-optic interfaces mounted on the RTM.

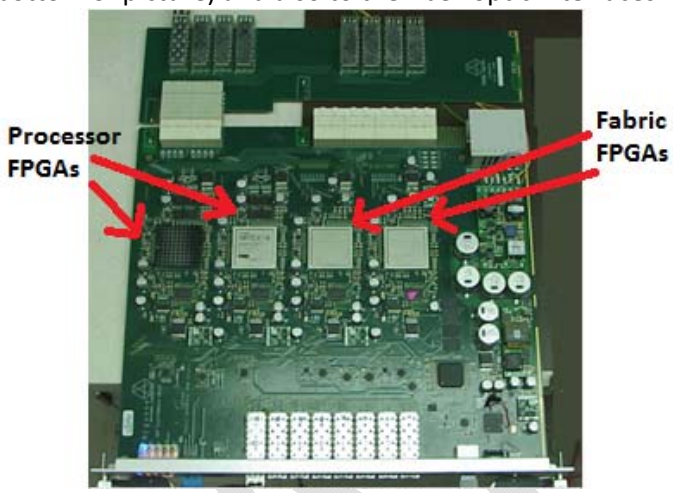

Figure 1 - Photo of prototype FLIC plus RTM.

The two large FPGAs in the center of the board, nearest the long white ATCA backplane connections, are called the ***fabric*** FPGAs. The ***processor*** FPGAs receive data though the front fiber-optic interfaces, process the data and push the results out the fiber-optic connections on the RTM. Selected subsets of data are transferred over the internal mesh of serial links from the ***processor*** FPGAs to the ***fabric*** FPGAs, who then build packets for transmission over the ATCA backplane to CPU cards, as shown in Figure 2.

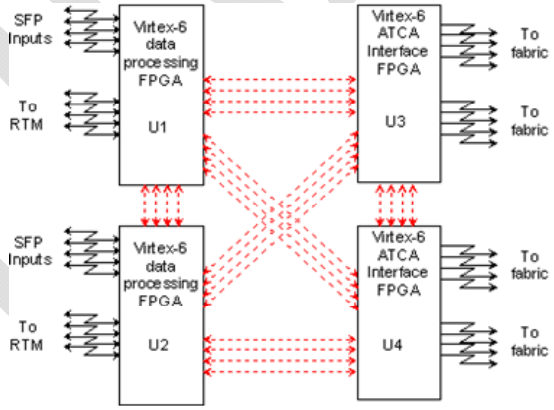

Figure 2 - Internal mesh of the FLIC.

Alternate FPGA Builds

For testing purposes, a third form of Virtex-6 firmware called the ***emulator*** has been developed that may be programmed into either or both ***processor*** FPGAs. The ***emulator*** firmware has the function of *driving* data out the fibers in the format expected by the ***processor*** firmware.

General Slow Control Structure of the FLIC

The FLIC implements five FPGAs on a shared slow control bus as shown in Figure 3. Access to the board for control or monitoring purposes is controlled by a small Management FPGA that processes read/write cycles from the PIC microcontroller. For compatibility with the ATCA standard an IPMC module connects to the PIC via a serial bus for sensor and monitoring requirements. At some future point the IPMC module may evolve to the point where the microprocessor of the IPMC may be the preferred control point, so the expansion bus of the IPMC is also connected to the Management FPGA.

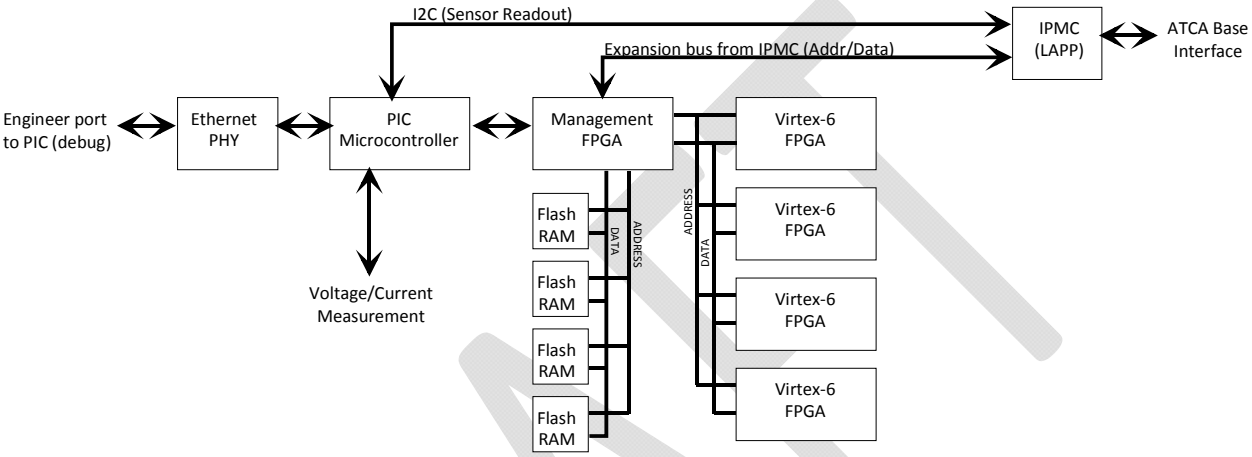

Figure 3 - Slow Control structure of FLIC

The Management FPGA firmware expects to receive single read/write transactions containing both address and data. The input side of the Management FPGA is a time-multiplexed address/data bus that is 16 bits wide.

Bus interface to Flash Memory

The Management FPGA implements a 24-bit address bus plus separate 16-bit data bus to the Flash RAMs. The address presented to the Flash RAMs is generated by first writing the upper bits of the address to a holding register inside the Management FPGA, then performing the data cycle to the Flash. A Chip Select code driven by the processor identifies the 'internal' versus the 'external' transactions. The Flash RAM interface uses +3.3V logic levels.

Bus interface to Virtex-6 FPGAs

The Management FPGA implements a 20-bit address bus plus separate 16-bit data bus to the Virtex-6 FPGA. The address presented to the FPGAs is generated by first writing the upper bits of the address to a holding register inside the Management FPGA, then performing the data cycle to the other FPGA. A Chip Select code driven by the processor identifies the 'internal' versus the 'external' transactions. The FPGA interface uses +2.5V logic levels as the Virtex-6 cannot directly connect to +3.3V logic levels; the Management FPGA performs level translation in addition to address/data routing.

Management FPGA Registers

The Management FPGA provides the bridge between the PIC microcontroller and the rest of the board. Four Processor Chip Select (PROC_CS) lines select which object on the board the PIC is talking to. Four main FPGAs (A, B, C & D) exist in addition to the Management FPGA. Main FPGAs 'A' and 'B' are physically wired to act as ***processor*** FPGAs that receive and process data in a pipeline fashion, whereas FPGAs 'C' and 'D' are physically wired to act as ***fabric*** FPGAs that connect to the ATCA backplane. The ***processor*** FPGAs may also be configured as ***emulator*** FPGAs that emulate the data stream generated by the rest of the FTK system, for self-testing.

PROC_CS	Device
0	FPGA A
1	FPGA B
2	FPGA C
3	FPGA D
4	Flash memory chip #1
5	Flash memory chip #2
6	Flash memory chip #3
7	Flash memory chip #4
8	Internal Management FPGA register
9-F	Currently unused

A pair of paged memory schemes differentiates access to the various board features through the slow control bus. The PIC processor external bus structure drives the architecture of the design. The PIC has a 16 bit bus that is used in multiplex address/data mode; thus, from the PIC's perspective, there is only a 16-bit address space. However, on the actual slow control bus, the address bus is 20 bits wide with a separate 16-bit data bus. Further paging games are requires in order to address the entire flash memory address space, and to access the large SRAMs associated with main FPGAs 'A' and 'B'.

A few registers are implemented within the Management FPGA, detailed on the following pages.

MGMT FPGA: Status Register (address 0)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	X	X	X	X	X	X	X	X	X	X	X	X	STAT	STAT	STAT	STAT

The four STAT bits are the STAT pins of the flash memory chips U34, U37, U160 and U161 respectively. These are used when programming the flash memories with information.

Flash Memory Sub-Architecture

Each flash memory chip consists of 128 'blocks' of data, each spanning 16k 16-bit words. The FLIC partitions each of the four flash memory chips into 8 partitions as shown in Figure 1. The main yellow area (41 blocks) contains sufficient memory (2,752,512 16-bit words) to hold the firmware image of one Virtex-6 FPGA. While we expect that in most applications of the FLIC FPGAs 'A' and 'B' will be identically programmed, and similarly that FPGAs 'C' and 'D' will be identically programmed, the flash is designed to allow each FPGA to have a unique image. This has already proven to be most valuable, as the FLIC on the test bench typically has the "data processing pipeline" code in FPGA 'A', but an "SSB Emulator" code in FPGA 'B' – because to date, no SSB board has been available for use at Argonne to test the FLIC.

FPGAs 'A' and 'B' both have four SRAM chips connected to them for module ID lookup when processing SSB data. Each SRAM's image is stored in the eight orange blocks of the flash map of Figure 1. After the Virtex-6 FPGAs are powered according to ATCA protocol, the Management FPGA may be commanded to copy the SRAM data from the flash to the actual SRAMs.

Other blocks in the flash memory are reserved for startup data private to the FLIC, but a number of spare blocks (colored white) are available. These may be used for board identification or tracking purposes if necessary.

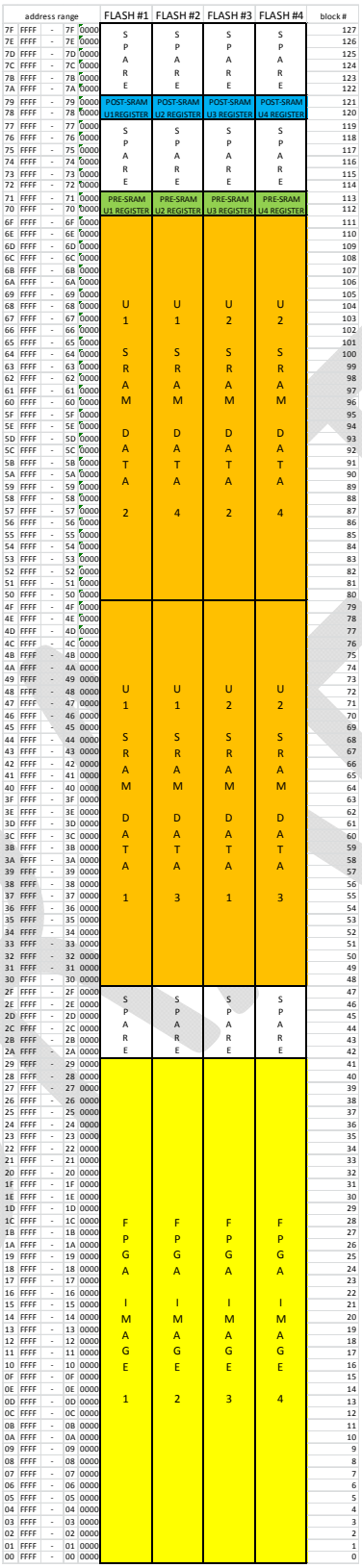

Figure 4 - Flash memory partitioning

MGMT FPGA: Control Register (address 1)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	SEL2	PWR	SEL1	Frst

- SEL2, if set, gives the Management FPGA control over the slow control bus to the other FPGAs. If clear, PIC accesses through chip selects 0,1,2,3 pass through to the slow control bus.
- SEL1 works the same as SEL2, except for the Flash memory data bus (and CS codes 4,5,6,7).
- The PWR bit, if set, informs the Management FPGA that the power has been turned on to the main FPGAs and that signals may be asserted on the inter-FPGA slow control bus.
- Frst, if set, asserts the RESET pin to all four flash memory chips.

The Control Register is used to manage the overall access to the slow control bus. The PWR bit is used to minimize leakage current through the un-powered Virtex-6 FPGAs during the time that only ATCA management power is provided to the board.

MGMT FPGA: Flash Memory Address Extension Register (address 2)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	FLASH ADDRESS BITS 23:16							

The data stored in the lower eight bits of the register at address 2 drives bits 23:16 of the address bus to the flash memory chips when these memories are accessed. This is due to the fact that the PIC processor only has a 16-bit address space, requiring a two-step access cycle.

MGMT FPGA: Inter-FPGA Address Extension Register (address 3)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	FPGA ADDRESS BITS 19:16			

The data stored in the lower eight bits of the register at address 2 drives bits 19:16 of the address bus to the other FPGAs when these memories are accessed. This is due to the fact that the PIC processor only has a 16-bit address space, requiring a two-step access cycle.

PROCESSING FPGA REGISTERS

The processing FPGA firmware operates as a data processing pipeline with multiple clock domains, as shown in Figure 5. In this drawing, two FPGAs are shown. At top left is an ***emulator*** FPGA that ***generates*** SSB data. The much larger portion of the drawing forms a block diagram of the ***processor*** FPGA architecture. This setup is what is used in bench testing.

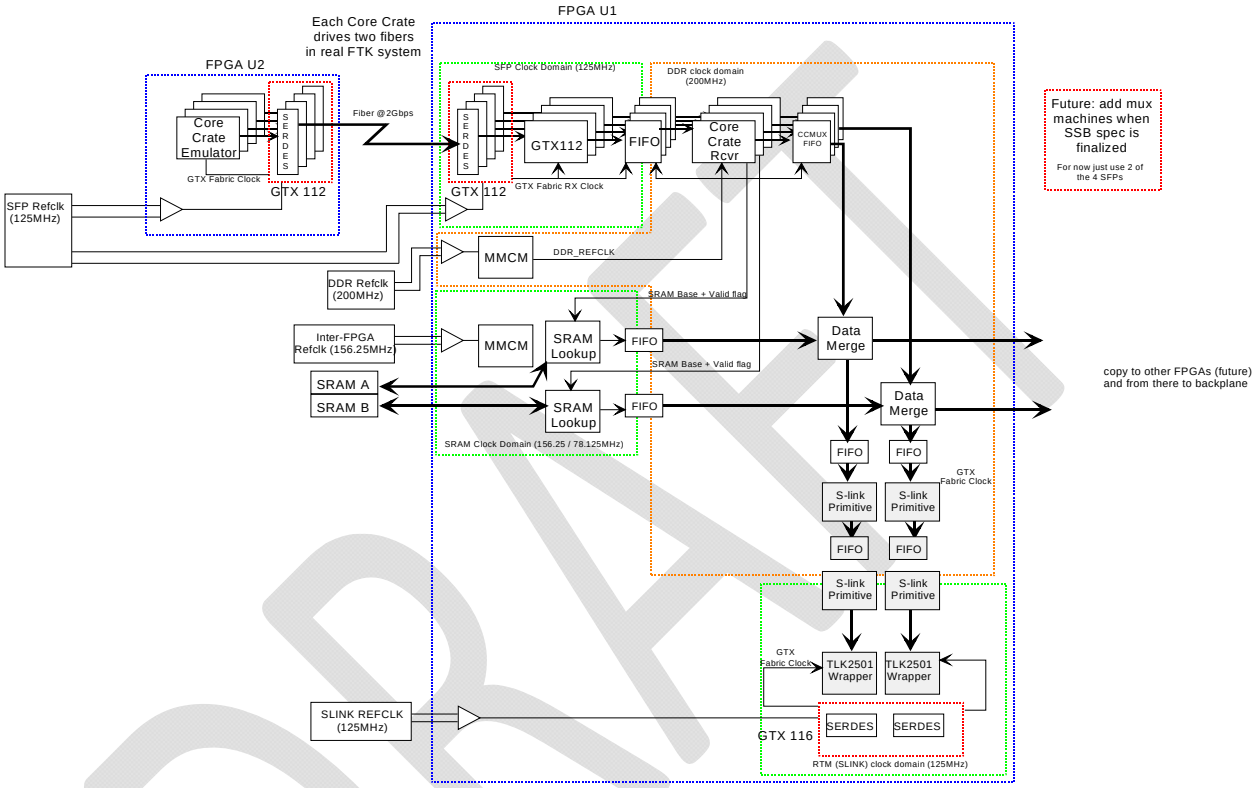

Figure 5 - FLIC Data Processing Pipeline Block Diagram

Data from the SSB (also known as a Core Crate) enters via SERDES block GTX112 and is immediately buffered into a FIFO. A Core Crate Receiver state machine, operating in a different clock domain, processes the events as they are received. A specific format has been agreed upon, described in Figure 5. The green *Record Header* and *Record Trailer* sections are always sent. The orange, yellow and beige sections constitute one *Track*, and any number of *Tracks* (including zero) may be sent in each *record*. The CoreCrateReceiver state machine uses the fixed values in the *Record Trailer* to synchronize to the incoming data; thus, the first record received is not processed. The *Tower* and *Sector Number* fields

Bit=> Word	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RH01	Region ID			0	1	1	0	1	0	0	1	1	0	1	0	0
RH02	Reserved															
RH03	Run Number - Bytes 3-2															
RH04	Run Number - Bytes 1-0															
RH05	Extended Level 1 ID - Bytes 3-2															
RH06	Extended Level 1 ID - Bytes 1-0															
RH07	Bunch Crossing ID - Bytes 3-2															
RH08	Bunch Crossing ID - Bytes 1-0															
RH09	Level 1 Trigger Type - Byte 3-2															
RH10	Level 1 Trigger Type - Byte 1-0															
RH11	Detector Event Type - Bytes 3-2															
RH12	Detector Event Type - Bytes 1-0															
RH13	NUM_TRACK_HI_PT_THRSH - Bytes 1-0															
RH14	NUM_TRACK_LO_PT_THRSH - Bytes 1-0															
TH1	TOWER			SSB_ID	1	1	0	1	0	1	1	0	1	0	0	
TH2	SECTOR_NUMBER[15:0]															
TH3	ROAD_ID[31..16]															
TH4	ROAD_ID[15..0]															
TH5	TRACK_D0[15..0]															
TH6	TRACK_Z0[15..0]															
TH7	TRACK_COTTH[15..0]															
TH8	TRACK_PHI0[15..0]															
TH9	TRACK_CHISQ[15..0]															
TH10	TRACK_CURV[15..0]															
TH11	TRACK_QUALITY[15..0]															
TH12	(Reserved for future use)[15..0]															
IBLa	RSV			ROW_WID	ROW_COORDINATE[11:0]											
IBLb	Typ	COL_WIDTH			COL_COORDINATE[11:0]											
PL0a	RSV			ROW_WID	ROW_COORDINATE[11:0]											
PL0b	Typ	COL_WIDTH			COL_COORDINATE[11:0]											
PL1a	RSV			ROW_WID	ROW_COORDINATE[11:0]											
PL1b	Typ	COL_WIDTH			COL_COORDINATE[11:0]											
PL2a	RSV			ROW_WID	ROW_COORDINATE[11:0]											
PL2b	Typ	COL_WIDTH			COL_COORDINATE[11:0]											
SAx0	Typ	AX_WIDTH			RSV	AX_COORDINATE[10:0]										
SSt0	Typ	ST_WIDTH			RSV	ST_COORDINATE[10:0]										
SAx1	Typ	AX_WIDTH			RSV	AX_COORDINATE[10:0]										
SSt1	Typ	ST_WIDTH			RSV	ST_COORDINATE[10:0]										
SAx2	Typ	AX_WIDTH			RSV	AX_COORDINATE[10:0]										
SSt2	Typ	ST_WIDTH			RSV	ST_COORDINATE[10:0]										
SAx3	Typ	AX_WIDTH			RSV	AX_COORDINATE[10:0]										
SSt3	Typ	ST_WIDTH			RSV	ST_COORDINATE[10:0]										
RTF1	Fixed Value 0x0F0F															
RTF2	Fixed Value 0xA5A5															
RTF3	Fixed Value 0xF0F0															
RTF4	Fixed Value 0x5A5A															
RTF5	Core Crate Status bits (format TBD)															
RTF6	Core Crate Status/Error bIts (format TBD)															

Figure 6 - Example of SSB (Core Crate) input format

Summary Table of Processor firmware registers

The following table provides a summary list of all the registers in the ***processor*** firmware with a short description of each. Detailed breakdowns of each register follow. Each register is tagged with an access type indicative of whether the register is

- Readable and writable (RW)
- Read-only (RO)
- Write-only (WO)

Write-only registers in the FLIC FPGAs are "pulsed control" registers. The pattern of set bits written to the register is translated into internal one-clock-tick wide pulses that are used for resets or triggers within the design. As the pulses occur before the write cycle completes, the register self-clears to zero by the end of the write cycle and thus useful data can be read from such registers.

Shading of cells indicates the status of the information in the following detail sections:
Gray **cells indicate registers where details have changed.**
Yellow **cells indicate registers for which detail information is not yet provided.**
Blue **cells indicate new registers added since the last revision of the document.**

Address	Mode	Name	Description
0x0000	RW	SLINK_CLOCK_CONTROL_REG	Controls external clock chip used as RTM SERDES reference
0x0001	RW	LED_REG	Controls front panel LED indicators
0x0002	RW	GENERAL_CTL_REG	General controls
0x0003	RW	SLINK_CTL_REG	Controls operation of RTM (S-Link) logic
0x0004	RW	SFP_CTL_REG	Controls operation of front panel (SFP) logic
0x0005 – 0x0008	RW	PRBS_CONTROL	Settings for pseudo-random number generators used in testing
0x0009	RW	SLINK_CTL2_REG	Secondary RTM (S-link) controls
0x000A	RW	COUNTER_CTL_REG	Overall control of diagnostic counters
0x000B	RW	ILA_MUX_CTL_REG	Controls multiplexed Internal Logic Analyzers.
0x000C – 0x000F	RW	TX_SEED	PRBS seeds for link test modes
0x0010 – 0x0011	RW	FORMAT_VERSION	Holds the S-Link format version value to put in all data
0x0012	RW	GTX113_CTL_REG	Control register for FPGA-to-FPGA serial link
0x0013	RW	GTX114_CTL_REG	Control register for FPGA-to-FPGA serial link
0x0014	RW	GTX115_CTL_REG	Control register for FPGA-to-FPGA serial link
0x0015 – 0x0016	RW	FLIC_STATUS_REG	FLIC status words to send over S-Link
0x0017 – 0x001E	RW	MON_FIFO_CTL_REG	Controls general purpose monitoring FIFO operation
0x001F	RW	HELD_RESETS_REG	For diagnostic use only
0x0020	RW	SFP_FIFO_PROG_EMPTY_THRESH_REG	FIFO threshold for flow control
0x0021	RW	SFP_FIFO_PROG_FULL_THRESH_REG	FIFO threshold for flow control

0x0022	RW	CCMUX_FIFO_PROG_EMPTY_THRESH_REG	FIFO threshold for flow control
0x0023	RW	CCMUX_FIFO_PROG_FULL_THRESH_REG	FIFO threshold for flow control
0x0024	RW	SRAM_FIFO_PROG_EMPTY_THRESH_REG	FIFO threshold for flow control
0x0025	RW	SRAM_FIFO_PROG_FULL_THRESH_REG	FIFO threshold for flow control
0x0026	RW	MERGE_FIFO_PROG_EMPTY_THRESH_REG	FIFO threshold for flow control
0x0027	RW	MERGE_FIFO_PROG_FULL_THRESH_REG	FIFO threshold for flow control
0x0028	RW	RTM_FIFO_PROG_EMPTY_THRESH_REG	FIFO threshold for flow control
0x0029	RW	RTM_FIFO_PROG_FULL_THRESH_REG	FIFO threshold for flow control
0x002A – 0x002B	RW	U3_L1_ID_MATCH_REG	Selects events to copy (spy buffer)
0x002C – 0x002D	RW	U4_L1_ID_MATCH_REG	Selects events to copy (spy buffer)
0x002E	RW	DDR_CONTROL_REG	Diagnostic use only
0x002F	RW	RESERVED	Unused, reserved for future use.
0x0100 – 0x0102	RO	CODE_REVISION, CODE_DATE_YYYY, CODE_DATE_MMDD	Firmware ID values
0x0103	RO	SFP_STATUS_REG	State machine status
0x0104	RO	RTM_STATUS_REG	State machine status
0x0105	RO	CCMUX_STATUS_REG	State machine status
0x0106	RO	SRAM_REFCLK_COUNTER	Frequency counters for clock diagnostics
0x0107	RO	DDR_REFCLK_COUNTER	Frequency counters for clock diagnostics
0x0108 – 0x010A	RO	GTX112_REFCLK_COUNTER, GTX112_TXCLK_COUNTER, GTX112_RXCLK_COUNTER	Frequency counters for clock diagnostics
0x010B – 0x010D	RO	GTX116_REFCLK_COUNTER, GTX116_TXCLK_COUNTER, GTX116_RXCLK_COUNTER	Frequency counters for clock diagnostics
0x010E	RO	UNUSED	Unused location
0x010F	RO	GTX116_RX_ERR_CNT_MUX	Multiplexed SERDES error counter
0x0110 – 0x011F	RO	MON_FIFO_DOUTs	Access to Monitor FIFOs
0x0120	RO	SLINK_CLK_STATUS_REG	
0x0121	RO	MON_FIFO_STATUS_REG	Empty/full status bits of FIFOs
0x0124 – 0x0127	RO	SSB_XOFF_CNT_REGs	Count of XOFFs sent to SSB
0x0128 – 0x012B	RO	SFP_FIFO_PROG_FULL_CNT_REGs	Count of how often this FIFO asked for flow control
0x012C – 0x012F	RO	CCMUX_FIFO_PROG_FULL_CNT_REGs	Count of how often this FIFO asked for flow control
0x0130 – 0x0133	RO	SRAM_FIFO_PROG_FULL_CNT_REGs	Count of how often this FIFO asked for flow control
0x0134 – 0x0137	RO	MERGE_FIFO_PROG_FULL_CNT_REGs	Count of how often this FIFO asked for flow control
0x0138 –	RO	RTM_FIFO_PROG_FULL_CNT_REGs	Count of how often this FIFO asked for flow

0x013B			control
0x013C – 0x013F	RO	SLINK_XOFF_CNT_REGs	Count of XOFFs received from S-Link
0x0140	RO	FIFO_EMPTY_REG	FIFO status flags
0x0141	RO	FIFO_PROG_EMPTY_REG	FIFO status flags
0x0142	RO	FIFO_PROG_FULL_REG	FIFO status flags
0x0143	RO	FIFO_FULL_REG	FIFO status flags
0x0144 – 0x0147	RO	GTX112_RX_ERROR_COUNTs	Count of errors in SSB data
0x0148	RO	DDR_STATUS_REG	
0x0200	WO	PULSED_CTL_REG_200	General purpose pulsed resets/triggers
0x0201	WO	PULSED_CTL_REG_201	General purpose pulsed resets/triggers
0x0202	WO	PULSED_CTL_REG_202	General purpose pulsed resets/triggers
0x0203	WO	PULSED_CTL_REG_203	General purpose pulsed resets/triggers
0x0204	WO	PULSED_CTL_REG_204	General purpose pulsed resets/triggers
0x0205	WO	PULSED_CTL_REG_205	General purpose pulsed resets/triggers
0x0206	WO	PULSED_CTL_REG_206	General purpose pulsed resets/triggers
0x0207	WO	PULSED_CTL_REG_207	General purpose pulsed resets/triggers
0x0208	WO	PULSED_CTL_REG_208	General purpose pulsed resets/triggers
0x0209	WO	PULSED_CTL_REG_209	General purpose pulsed resets/triggers
0x020A	WO	PULSED_CTL_REG_20A	General purpose pulsed resets/triggers
0x020B	WO	PULSED_CTL_REG_20B	General purpose pulsed resets/triggers
0x020C	WO	PULSED_CTL_REG_20C	General purpose pulsed resets/triggers
0x020D	WO	PULSED_CTL_REG_20D	General purpose pulsed resets/triggers
0x020E	WO	PULSED_CTL_REG_20E	General purpose pulsed resets/triggers
0x020F	WO	PULSED_RESETS_REG	General purpose pulsed resets/triggers
0x0300	RW	SRAM_ADDRESS_EXTENSION	Address extension holding register
0x0310 – 0x031F	RO	PIPELINE1_DIAG_COUNTERS	Block of 16 diagnostic counters associated with pipeline #1
0x0320 – 0x032F	RO	PIPELINE2_DIAG_COUNTERS	Block of 16 diagnostic counters associated with pipeline #2
0x0330 – 0x033F	RO	PIPELINE3_DIAG_COUNTERS	Block of 16 diagnostic counters associated with pipeline #3
0x0340 – 0x035F	RO	PIPELINE4_DIAG_COUNTERS	Block of 16 diagnostic counters associated with pipeline #4
0x10000 – 0x1FFFF	RW	SRAM1 ACCESS WINDOW	
0x20000 – 0x2FFFF	RW	SRAM2 ACCESS WINDOW	
0x30000 – 0x3FFFF	RW	SRAM3 ACCESS WINDOW	
0x40000 – 0x4FFFF	RW	SRAM4 ACCESS WINDOW	

PROCESSOR FPGA: ADDRESS 0x0000 : SLINK_CLOCK_CONTROL_REG

The SLINK_CLOCK_CONTROL register allows to user to control the pins of the clock generator that provides the reference clock for all S-LINK (RTM) SERDES links in both processing FPGAs. These are the SERDES links that drive the rear transition module.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	X	CLOCK RATE INDEX		

USAGE

This register is used in conjunction with the PULSED_CTRL register located at address 0x020E. The Clock Rate Index value provides eight pre-defined control pin settings for the expected use cases:

Setting	Clock Rate	RTM SFP rate	Notes
0	62.50MHz	1Gbps	Only available in “slow” build.
1	125.00MHz	2Gbps	Only available in “slow” build.
2	156.25MHz	N/A	Rate associated with 10GbE
3	187.50MHz	3Gbps	*Beyond S-Link Specifications*
4	200.00MHz	N/A	Frequency used for DDRs
5	*250.00MHz*	*4Gbps*	*Performance not guaranteed*
6	*312.50MHz*	*5Gbps*	*Performance not guaranteed*
7	*375.00MHz*	*6Gbps*	*Performance not guaranteed*

IMPORTANT NOTES

Setting the Clock Rate Index value will change the reference clock rate provided to the GTX blocks of the Virtex-6 by the clock generator chip to the desired frequency, but this does ***not*** mean that the GTX will necessarily work at the clock rate selected. The GTX blocks use an internal phase locked loop (PLL) that has a limited range of operation. The frequency multiply/divide settings, determined at compile time and not at run time, specify what frequencies are possible. For the GTX blocks as defined in the FLIC, there are two sets of settings in the User Constraint File (UCF), the “slow” and the “fast”, and there are two separately maintained firmware tags for these two speed ranges.

GENERAL USAGE

The firmware within the FPGAs of the FLIC implements the S-Link protocol using VHDL obtained from CERN. This firmware is not certified to operate at rates above 2Gbps. Operation of the S-Link at higher speeds is not guaranteed and has not been tested. To set a new clock speed, the user sets the Clock Rate Index to the desired value then performs a write to the PULSED_CTRL register located at address 0x020E to initiate a state machine that resets the external clock generator chip and sets the new frequency.

DEFAULT VALUE AT POWER UP

At power up the register has the value 0x0001, which should set the clock to 125MHz. It is recommended that software perform a clock frequency setting operation as part of normal initialization to be certain that the clock generator has been set to the desired frequency.

PROCESSOR FPGA: ADDRESS 0x0001 : LED_REG

Generic diagnostic register allowing the user to play with two of the board's LEDs.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	X	X	LED5	LED4

USAGE

Until specific functions are associated with the two front panel LEDs associated with U1, this register allows manual control.

DEFAULT VALUE AT POWER UP

At power-up the register initializes to the value zero, turning both LEDs off.

PROCESSOR FPGA: ADDRESS 0x0002 : GENERAL_CONTROL_REG

Generic control register allowing the user to override automatic settings.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	RST SRC	G116 RTX	G116 RRX	G115 RTX	G115 RRX	G114 RTX	G114 RRX	G113 RTX	G113 RRX	G112 RTX	G112 RRX	Merge En	SRAM Access	ILA SEL	CCR EN	CLK

BIT DESCRIPTIONS

- Bit 0, if clear, leaves control of the external clock chips to the state machines. Otherwise, if the bit is set, this enables use of the Clock Control Register for manual control.
- Bit 1, if set, enables data processing in the Core Crate Receiver machines.
- Bit 2 selects which SRAM lookup data is sampled for the General ILA
- Bit 3, if set, allows the SRAM state machine to drive the address buses to the external SRAMs. If clear, access to the SRAM via mapped slow control bus addresses is enabled.
    - Bits 3:2 of this register are connected to bits 90:89 of the general purpose ILA.
- Bit 4, if set, enables data processing in the Merge machines.
- Bits 6:5 provide the manual TX and RX resets for the frame state machines in GTX112 (front)
- Bits 8:7 provide the manual TX and RX resets for the frame state machines in GTX113 (internal)
- Bits 10:9 provide the manual TX and RX resets for the frame state machines in GTX114 (internal)
- Bits 12:11 provide the manual TX and RX resets for the frame state machines in GTX115 (internal)
- Bits 14:13 provide the manual TX and RX resets for the frame state machines in GTX116 (RTM)
- Bit 15, if clear, means that the RTX and RRX bits of this register are manual resets to the frame generator (TX) and frame checker (RX) blocks for the GTX blocks. If bit 15 is set, the resets for these units are derived from control signals from the SERDES cores.

USAGE NOTES

Each GTX block within the FPGA has wrapped around it “PRBS frame generator” and “PRBS frame checker” state machines. The reset bits here in the GENERAL_CONTROL register are logically ORed with other bits from the various PULSED_CTRL registers to create the reset signal to the PRBS state machines. Bit 15 of the GENERAL_CONTROL register, if set, disables register control of these resets and ties the resets of the PRBS machines to the internal GTX reset signals; generally, this mode of operation is not used and not recommended.

In most GTX implementations of U1 the actual TX data is driven by a multiplexer where PRBS data is but one of the options. Each GTX has its own controls to determine how many multiplexer selections there are, found in other registers. The PRBS data generator is designed so that, while reset, it sends K28.5 comma characters.

DEFAULT VALUE AT POWER-UP: 0x0000.

PROCESSOR FPGA: ADDRESS 0x0003 : SLINK_CTL_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SLINK Test Pattern Enable				SLINK Reset Controller GO				SLINK TX Mux Sel				RTM TDIS			

BIT DESCRIPTIONS

- Bits 3:0 directly drive the TDIS lines of the four SFP modules of the rear transition module driven by the FPGA. Each bit, if ***set***, will ***disable*** the SFP unit.
- Bits 7:4 control the operation of the TX data path mux in the GTX116 logic. If the Mux Sel bit is ***clear*** *(0)*, the GTX is set to send pseudo-random test pattern data. If the bit is ***set*** *(1)*, GTX data comes from the CERN SLINK wrapper.
- Bits 10:8 are the 'GO' bits that, when set, enable the SLINK Reset Controller state machine to perform the SLINK initialization process. The SLINK logic won't do anything until the 'GO' bit is set. There is one bit per GTX in the GTX116 quad.
- Bits 15:12 are the Test Pattern Enable bits that allow the SLINK logic as given to us by CERN to send the SLINK Test Pattern.
    - *The Test Pattern Enable and 'GO' bits for a given link are mutually exclusive; don't set both at the same time.*

USAGE NOTES:

Normally this register is changed from 0x0000 to 0x00F0 by user software to select S-Link data prior to initializing communication with any S-Link receiver board. After the physical S-Link connection is present, then it is normally necessary to change the value first to 0x0FF0 to enable the reset controller to reset the CERN S-Link core, and then change the value back to 0x00F0 to start transmitting data. This is because a reset of the CERN core is necessary after the S-Link receiver stops asserting the "link down" status to remove the local "link down" status inside the FLIC.

In normal operation the upper four bits are never set, save for when some CERN engineer requests them to be set for S-Link specific diagnosis. For FLIC PRBS testing, the CERN test pattern is ***never*** used; the FLIC makes its own PRBS data stream of a different format for link testing.

DEFAULT VALUE AT POWER-UP : 0x0000. This means that all SFP transmitters are enabled, the TX Mux is set to PRBS data and the CERN SLINK wrapper is held reset.

PROCESSOR FPGA: ADDRESS 0x0004 : SFP_CTL_REG

This register provides controls specific to the SFP fiber interfaces of the front panel, connected to GTX block 112 within the FPGA.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	GTX112 TX MUX CTL				**T**ransmitter **DIS**able (TDIS)			

BIT DEFINITIONS

- Bits 15:8 are unused.
- Bits 7:4 are used to select the type of data transmitted by the FLIC to the SSB. Bits 7:4 control the data in front panel SFP links 3:0 of U1, respectively.
    - If a given TX MUX bit is ***set***, the FLIC sends XON / XOFF control data to the SSB.
    - If a given TX MUX bit is ***clear***, the FLIC sends PRBS test data.
- Bits 3:0 are the **T**ransmitter **DIS**able, or TDIS bits. Each TDIS bit, if set high, disables the associated front panel fiber transmitter. The order of these bits is that bit 0 is the leftmost SFP of the four connected to a given FPGA, as viewed looking into the front panel; bit 3 is the right-most.

USAGE

Normally this register is left untouched. The TDIS bits are only used to disable transmitters for diagnostic purposes or to minimally reduce power consumption by disabling unused SFP modules. The user may opt to clear bits 7:4 during board testing to send PRBS data.

DEFAULT VALUE AT POWER-UP : 0x00F0. This ***enables*** all the SFP modules, so the user doesn't need to do anything to send or receive data. Similarly, all SFP links are set to be sending SSB flow control data, the default for FTK usage.

PROCESSOR FPGA: ADDRESS 0x0005 – 0x0008 : PRBS CONTROL REGISTERS

This set of four registers defines the (Pseudo-Random Bit Sequence) PRBS control parameters. A PRBS generator is available to drive a programmable data sequence out any SERDES link. A matching PRBS receiver will lock on to the pattern and compare received data to transmitted data for bit-error-rate-testing (BERT).

REGISTER 0x0005: NUMBER OF COMMAS AFTER RESET

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	INITIAL NUMBER OF COMMAS AFTER RESET															

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0020.

REGISTER 0x0006: NUMBER OF WORDS TO SEND BEFORE INSERTING COMMA(S)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Number of words to send before inserting comma character(s)															

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0040.

REGISTER 0x0007: NUMBER OF COMMAS TO SEND IN COMMA BREAKS

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	UNUSED												# of commas			

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0002.

REGISTER 0x0008: TOTAL NON-COMMA PATTERN LENGTH BEFORE PATTERN RESTART

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Number of words to send before restarting PRBS sequence.															

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0100.

The pseudo-random sequence is generated using a shift register with exclusive-or gates. In the current version of the *processor* code, four PRBS generators and four PRBS receivers are connected to the four SERDES units associated with the four front panel SFP connections. The seed values for each PRBS are different, stored in registers at addresses 0x000C, 0x000D, 0x000E and 0x000F. The default seeds are 0x0135, 0x1234, 0x5678 and 0xF18A. A PRBS spreadsheet in the code repository may be used to generate the expected data stream for any seed.

Understanding the PRBS data sequence

The PRBS design encoded within the FLIC is a self-seeding design. Upon reset, the PRBS generator sends a fixed set of comma characters for initialization then falls into an endless sequence of data. That sequence is defined by the registers at addresses 6, 7 & 8. The sequence is defined as follows:

- A set of three words of value 0x0000 defines a PRBS pattern block.
  - The first word after the three zeroes is used to seed a PRBS generator in the receiver.
- A number of PRBS words, including the seed, as defined by the value in register 6, are sent.
- After the set of PRBS words are sent, a block of commas is sent, the number defined by the value in register 7.
- The PRBS-comma-PRBS-comma… sequence continues until the total number of PRBS words as defined in register 8 have been sent.
- After the total length requirement is satisfied, a new set of three zeroes is sent and then data continues. The PRBS data continues to be generated in the transmitter so that each block is unique.

On the receiver end, the first word after each block of three 0x0000 words is used as the seed to the receiver's PRBS generator. Each word after the seed is then compared against the data being received and an error flag is generated on any mismatch. An error is also flagged if the number of words with the value 0x0000 is not exactly three. Should there be an error in the transmission of the seed value, all values in the block will fail to match. To avoid an endless stream of errors stemming from one error in the seed value, the PRBS test sequence re-seeds regularly.

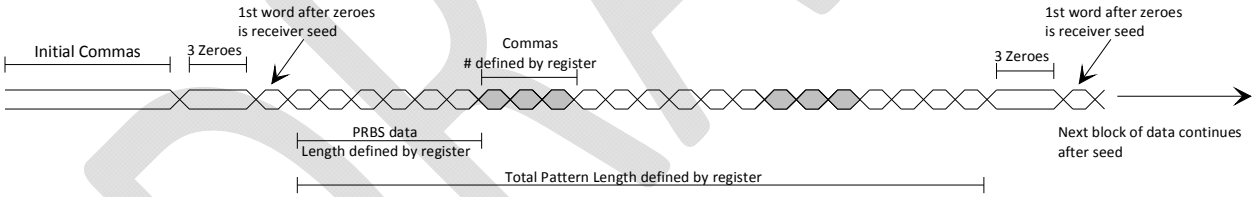

Figure 7 - PRBS data sequence.

PROCESSOR FPGA: ADDRESS 0x0009 : SLINK_CTL2_REG

This register provides ancillary controls associated with the SFP links of the rear transition module (GTX116).

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	FORCE LINK UP			

BIT DEFINITIONS

- Bits 15:4 are unused.
- Bit 3:0 affect the processing of data for each of the four RTM links. If set, the LDOWN* (Link DOWN) status from the S-Link logic is ignored and the data in the RTM FIFO is processed as if the S-Link was up.

USAGE

Normally this register is left untouched, but the bits may be set to allow operation of the FLIC irrespective of the status of the S-Link receiver for diagnostic purposes.

DEFAULT VALUE AT POWER-UP : 0x0000. This allows normal S-Link operation.

PROCESSOR FPGA: ADDRESS 0x000A : COUNTER_CTL_REG

This register provides some general purpose bits to reset and/or control the mode of various diagnostic counters within the FLIC.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	RST	MODE	RST	MODE	RST	MODE	RST	MODE	RST	MODE	RST	MODE	X	X	X	X
	PIPELINE		GTX112		GTX113		GTX114		GTX115		GTX116		X	X	X	X

A variety of diagnostic counters are implemented within the FLIC, grouped based upon what section of the logic they monitor. On a group by group basis, the RST and MODE bits are used to control all counters within that group.

- If the RST bit is set, all counters within the group are held reset. If the RST bit is clear, the counter is free to count.
- When enabled to count, the MODE bit sets the counter mode:
  - If the MODE bit is clear, the counter simply increments whenever the signal being monitored is high.
  - If the MODE bit is set, the counter provides a *rate* measurement of how fast the counter is counting (e.g. Hz, MHz, etc.).
  - For rare events, MODE clear is usually preferred; when looking at clock rates or other common events, setting the MODE bit to see how often the event is occurring is usually chosen.

Counters in each group

The PIPELINE group contains the SRAM_REFCLK_COUNTER and DDR_REFCLK_COUNTER. These counters are typically used with the MODE bit high, to measure the speed of the SRAM and DDR clocks. The rate is sampled every microsecond so the counter value will read the frequency of the clock in MHz.

The GTX112 group contains the counters for the GTX112 REFCLK, TXCLK and RXCLK. These are normally used with MODE high, to measure the clock frequencies within this block. The rate is sampled every microsecond so the counter value will read the frequency of the clock in MHz. The GTX113, GTX114, GTX115 and GTX116 groups are handed identically.

PROCESSOR FPGA: ADDRESS 0x000B : ILA_MUX_CTL_REG

Controls operation of the multiplexed latches used to capture data prior to connection to the Chipscope internal logic analyzer.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	SRAM MUX SEL		PIPELINE MUX SEL		GTX 116 MUX SEL		GTX 115 MUX SEL		GTX 114 MUX SEL		GTX 113 MUX SEL		GTX 112 MUX SEL	

BIT DEFINITIONS

Each bit pair is associated with a different Chipscope ILA used within the FLIC firmware. As there are four processing pipelines within the FPGA, and also four SERDES links within a GTX quad, it is natural to use a two bit code per ILA for selection.

USAGE

Set as desired to set up internal monitoring throughout the FPGA. Typically the GTX mux value will be set the same as the Pipeline mux value during FTK use so that the entire pipeline from SFP input to RTM output may be viewed. The Pipeline mux selection is common to the Core Crate Receiver, Data Merge and SLINK_PRIMITIVE machines within each pipeline.

DEFAULT VALUE AT POWER-UP : 0x0000.

PROCESSOR FPGA: ADDRESSES 0x000C through 0x000F : TX_SEED REGISTERS

These registers define the starting (seed) value to use in the PRBS generators (frame generators). The register at address 0x00C defines the seed for link 0 of GTX112 and also for link 0 of GTX116. TX_SEED0 defaults at power-up to 0x0135; TX_SEED1 to 0x1234, TX_SEED2 to 0x5678 and TX_SEED3 to 0xF18A.

PROCESSOR FPGA: ADDRESSES 0x0010 & 0x0011 : FORMAT VERSION

The registers at addresses 0x0010 (low half) and 0x0011 (high half) are used to store the 32-bit format version that the FLIC transmits in the data header out the S-Link.

DEFAULT VALUE AT POWER-UP : 0x03010000.

PROCESSOR FPGA: ADDRESSES 0x0012 through 0x0014 : GTXnnn_CTL_REG

This register provides controls specific to the SFP fiber interfaces of the front panel, connected to GTX blocks 113 through 115 within the FPGA.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	ENABLE_TIMING_TAGS				Enable FIFO			

BIT DEFINITIONS

- Bits 15:8 are unused.
- Bits 7:4 are used to enable insertion of timing tag bits into the receiving FIFO, for engineering diagnostic use only.
- Bits 3:0 select whether each SERDES line within the GTX block sends data from the TX-side FIFO (bit set), or sends PRBS test data (bit clear).

USAGE

Typically this register is written after link integrity of the FPGA-to-FPGA link has been established by checking the PRBS data reception. After link integrity is verified, then bits 3:0 are set to enable transmission of normal data. The link can be set to send nothing but comma characters all the time by clearing the Enable FIFO bit in this register (to send PRBS data) and then additionally setting the appropriate bit in the GENERAL_CTL register to hold the PRBS machine in reset.

DEFAULT VALUE AT POWER-UP : 0x0000. This sets all four links of the GTX block to be sending PRBS test data.

.

PROCESSOR FPGA: ADDRESSES 015, 016 : FLIC Status Values

These registers define two “FLIC Status Words” that are appended to the end of every event that passes through the FLIC. At some future point the status values will be redefined to contain specific live status bits indicative of module status, but for now they’re merely dummy values useful only to place two known words into the data stream.

DEFAULT VALUE AT POWER-UP : 0x0000, 0x0000.

PROCESSOR FPGA: ADDRESSES 017 through 01E : MON_FIFO_CTL_REGs

Eight "Monitor FIFOs" allow manual capture of data at various stages of the design. These FIFOs all fill using the clock appropriate to the section of the design they monitor, but all read out using the slow control clock. Each Monitor FIFO has an associated control register to allow selection of what the input is or when a capture occurs.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	WE mode		src select	

BIT DEFINITIONS

- Bits 15:2 are unused.
- Bits 1:0 select which of the four pipelines within the processing FPGA is being monitored by the given MON_FIFO. This applies to MON_FIFOs 0,1,2 & 3. MON_FIFOs 4-7 are currently unused.
    - MON_FIFO 0 monitors data as it falls out of the CCMUX FIFO.
    - MON_FIFO 1 monitors data as it falls out of the SRAM FIFO.
    - MON_FIFO2 monitors data as it falls out of the MERGE FIFO.
    - MON_FIFO3 monitors data entering the RTM FIFO.
- Bits 3:2 select various writing modes for MON_FIFO 0 ***only***.
    - 00: capture always
    - 01: capture when data is tagged for inter-fpga transfer to U3.
    - 10: capture when data is tagged for inter-fpga transfer to U4.
    - 11: capture only if CoreCrateRcvr has flagged an error; stop when Event-End tag falls out.
- All other MON_FIFOs write all the time.

USAGE

Different Monitor FIFOs have been connected to various points in the processing pipeline. Each FIFO's position in the pipeline in fixed with a multiplexer to select between the pipelines. These registers, on a FIFO by FIFO basis, select which of the pipelines the given FIFO will monitor.

Each of the Monitor FIFOs is reset by writing the appropriate bit to the Pulsed Control register at address 0x020C.

DEFAULT VALUE AT POWER-UP : 0x0000. This sets all Monitor FIFOs to be monitoring pipeline 0.

PROCESSOR FPGA: ADDRESS 0x001F : HELD_RESETS_REG

General purpose control register, specifically aimed at resets. Bits set within this register are typically ORed with Pulsed Control bits to allow to user to hold some section of logic reset, as opposed to applying a pulsed reset that is immediately released.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	G116 FREAD	G116 FIFO	SLINK PRIM	MERGE	Hola Core	TLK	SRAM B	SRAM A	CCMUX FIFO resets				Core Crate Rcvr Resets			

BIT DEFINITIONS

- Bits 3:0 are pulsed resets for four Core Crate Rcvr blocks. The DDR-domain ILA monitors these bits as ILA bit 88 (section selected by ILA mux controls).
- Bits 7:4 are pulsed resets for the four CCMUX FIFOs.
- Bit 8 resets SRAM machine A; bit 9 resets SRAM machine B.
- Bit 10 resets the TLK reformatter logic from CERN in all four GTX116 copies.
- Bit 11 resets the Hola Core (S-link) logic taken from CERN in all four GTX116 copies.
- Bit 12 resets all Merge state machines and all Merge FIFOs.
- Bit 13 resets all SLINK_PRIMITIVE machines.
- Bit 14 resets all GTX 116 event FIFOs.
- Bit 15 resets all GTX 116 FIFO reader machines.

PROCESSOR FPGA: ADDRESS 0x0020 : SFP_FIFO_PROG_EMPTY_THRESH

The SFP_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the front panel SFP input FIFO, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SFP FIFO PROGRAMMABLE EMPTY THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Empty flag. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-empty at ½ the depth of the FIFO and writing 0xC000 sets the prog-empty point at ¾ of the FIFO's depth.

USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0400. This is ¼ full.

PROCESSOR FPGA: ADDRESS 0x0021 : SFP_FIFO_PROG_FULL_THRESH

The SFP_FIFO_PROG_FULL_THRESH register sets the Programmable Full threshold of the front panel SFP input FIFO, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SFP FIFO PROGRAMMABLE FULL THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Full flag, causing the FLIC to assert the XOFF message to the SSB. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-full at ½ the depth of the FIFO and writing 0xC000 sets the prog-full point at ¾ of the FIFO's depth.

USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0C00. This is ¾ full.

PROCESSOR FPGA: ADDRESS 0x0022 : CCMUX_FIFO_PROG_EMPTY_THRESH

The CCMUX_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the CoreCrateRcvr and Merge state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	CCMUX FIFO PROGRAMMABLE EMPTY THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Empty flag. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-empty at ½ the depth of the FIFO and writing 0xC000 sets the prog-empty point at ¾ of the FIFO's depth.

USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0400. This is ¼ full.

PROCESSOR FPGA: ADDRESS 0x0023 : CCMUX_FIFO_PROG_FULL_THRESH

The CCMUX_FIFO_PROG_FULL_THRESH register sets the Programmable Empty threshold of the FIFO between the CoreCrateRcvr and Merge state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	CCMUX FIFO PROGRAMMABLE FULL THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Full flag, causing the FLIC to assert the XOFF message to the SSB. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-full at ½ the depth of the FIFO and writing 0xC000 sets the prog-full point at ¾ of the FIFO's depth.

USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0C00. This is ¾ full.

PROCESSOR FPGA: ADDRESS 0x0024 : SRAM_FIFO_PROG_EMPTY_THRESH

The SRAM_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the SRAM Lookup and Merge state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SRAM FIFO PROGRAMMABLE EMPTY THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Empty flag. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-empty at ½ the depth of the FIFO and writing 0xC000 sets the prog-empty point at ¾ of the FIFO's depth.

USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0400. This is ¼ full.

PROCESSOR FPGA: ADDRESS 0x0025 : SRAM_FIFO_PROG_FULL_THRESH

The SRAM_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the SRAM Lookup and Merge state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SRAM FIFO PROGRAMMABLE FULL THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Full flag, causing the FLIC to assert the XOFF message to the SSB. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-full at ½ the depth of the FIFO and writing 0xC000 sets the prog-full point at ¾ of the FIFO's depth.

USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0C00. This is ¾ full.

PROCESSOR FPGA: ADDRESS 0x0026 : MERGE_FIFO_PROG_EMPTY_THRESH

The MERGE_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the Merge and SLINK_PRIMITIVE state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	MERGE FIFO PROGRAMMABLE EMPTY THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Empty flag. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-empty at ½ the depth of the FIFO and writing 0xC000 sets the prog-empty point at ¾ of the FIFO's depth.

USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0400. This is ¼ full.

PROCESSOR FPGA: ADDRESS 0x0027 : MERGE_FIFO_PROG_FULL_THRESH

The MERGE_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the Merge and SLINK_PRIMITIVE state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	MERGE FIFO PROGRAMMABLE FULL THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Full flag, causing the FLIC to assert the XOFF message to the SSB. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-full at ½ the depth of the FIFO and writing 0xC000 sets the prog-full point at ¾ of the FIFO's depth.

USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0C00. This is ¾ full.

PROCESSOR FPGA: ADDRESS 0x0028 : RTM_FIFO_PROG_EMPTY_THRESH

The RTM_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the SLINK_PRIMITIVE and S-Link controller state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	RTM FIFO PROGRAMMABLE EMPTY THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Empty flag. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-empty at ½ the depth of the FIFO and writing 0xC000 sets the prog-empty point at ¾ of the FIFO's depth.

USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0400. This is ¼ full.

PROCESSOR FPGA: ADDRESS 0x0029 : RTM_FIFO_PROG_FULL_THRESH

The RTM_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the SLINK_PRIMITIVE and S-Link controller state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	MERGE FIFO PROGRAMMABLE FULL THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Full flag, causing the FLIC to assert the XOFF message to the SSB. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-full at ½ the depth of the FIFO and writing 0xC000 sets the prog-full point at ¾ of the FIFO's depth.

USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0C00. This is ¾ full.

PROCESSOR FPGA: ADDRESS 0x002A/0x002B : U3_L1_ID_MATCH_REG

The U3_L1_ID_MATCH register contains a bit-mask that is bit-by-bit ANDed with the Level 1 ID value received from the SSB each event. If the bit-by-bit AND operation results in a non-zero value, the event is selected for copying over the inter-FPGA SERDES link to Fabric Processor U3.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SELECTION BITMASK BITS 15:0 (address 0x002A)															
RW	SELECTION BITMASK BITS 31:16 (address 0x002B)															

BIT DEFINITIONS

Each bit is individually ANDed with the same order bit in the Level 1 ID value of the incoming event. The results of the 32 AND operations are ORed together to create a single "tag" bit that marks whether the event is to be copied to the Fabric FPGA for eventual transfer to a processor in the ATCA shelf the FLIC resides in.

USAGE

Set as desired. Bear in mind that the Level 1 ID is a *counter*, so setting low bits will select many events. For example, a value of 0x0000 in address 0x002B and a value of 0x0001 in address 0x002A will copy every other event. However, setting address 0x002B to 0 and setting address 0x002A to 0x0010 will only copy every 16th event.

As the upper eight bits of the Level 1 ID have somewhat special meaning, at some future point the match logic may be expanded to allow other options, but it should *never* be assumed that any kind of lookup table that would allow arbitrary selection of specific L1 ID values will *ever* be implemented. The timing of such a function is impossible.

DEFAULT VALUE AT POWER-UP : 0x00000000. No events will be copied.

PROCESSOR FPGA: ADDRESS 0x002C/0x002D : U4_L1_ID_MATCH_REG

The U4_L1_ID_MATCH register contains a bit-mask that is bit-by-bit ANDed with the Level 1 ID value received from the SSB each event. If the bit-by-bit AND operation results in a non-zero value, the event is selected for copying over the inter-FPGA SERDES link to Fabric Processor U4.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SELECTION BITMASK BITS 15:0 (address 0x002A)															
RW	SELECTION BITMASK BITS 31:16 (address 0x002B)															

BIT DEFINITIONS

Each bit is individually ANDed with the same order bit in the Level 1 ID value of the incoming event. The results of the 32 AND operations are ORed together to create a single "tag" bit that marks whether the event is to be copied to the Fabric FPGA for eventual transfer to a processor in the ATCA shelf the FLIC resides in.

USAGE

Set as desired.

DEFAULT VALUE AT POWER-UP : 0x00000000. No events will be copied.

PROCESSOR FPGA: ADDRESSES 0x2E : DDR_CONTROL_REG

Engineer-only register used to control DDR memory test firmware.

PROCESSOR FPGA: ADDRESS 0x2F : Unused

PROCESSOR FPGA: ADDRESSES 0x30 – 0x35 : PIPELINE_COUNTER_CONTROLS

Reserved locations for overall control registers for full diagnostic counters across all pipelines. ***Not yet implemented.***

PROCESSOR FPGA: ADDRESS 0x100 : CODE_REVISION

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Major Revision				Minor Revision				Sub-Revision				Day Index			

The CODE_REVISION register provides a location to read the current version of the FLIC firmware. This register is changed when the firmware is modified to allow the user to determine if the board contains the latest revision of firmware. The current value as of November 6, 2014 is 0x0105 (Version 0.1.0.5).

PROCESSOR FPGA: ADDRESS 0x101 : CODE_DATE_YYYY

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Year of last code revision															

The CODE_DATE_YYYY register provides a location to read the date, as stored by the firmware engineer, of the version of code within the FPGA.

PROCESSOR FPGA: ADDRESS 0x102 : CODE_DATE_MMDD

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Month of last code revision								Day of month of last code revision							

The CODE_DATE_MMDD register provides a location to read the date, as stored by the firmware engineer, of the version of code within the FPGA.

PROCESSOR FPGA: ADDRESS 0x103 : SFP_STATUS_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	LOS				MOD_PRESENT				RATESEL				TFAULT			

The SFP status register provides four bit-fields indicative of the state of the four front panel SFP modules connected to the FPGA. Within a four-bit group, the most significant bit is associated with the SFP furthest to the right of the group on the front panel when the board is in its normal operating orientation in the ATCA shelf.

The LOS (**L**oss **O**f **S**ignal) field reads back the loss of signal indicator from each of SFP0 through SFP3 (bit 12: SFP0, 13:1, 14:2, 15:3). The LOS bit is set if the receiving optics of the given SFP fails to detect an optical signal.

The MOD_PRESENT lines are pulled up by resistors on the FLIC but pulled down by the SFP module when the module is inserted; thus 0 is “module present” and 1 is “module absent”.

The RATESEL bits are reserved for identification of multi-speed transceivers.

The TFAULT bits, if high, indicate a transmitter fault. TFAULT is an open-collector signal requiring a pullup resistor on the FLIC to operate.

PROCESSOR FPGA: ADDRESS 0x104 : RTM_SFP_STATUS_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	LOS				MOD_PRESENT				RATESEL				0	0	0	0

The RTM SFP status register provides four bit-fields indicative of the state of the four rear transition module SFP units connected to the FPGA. Within a four-bit group, the most significant bit is associated with the SFP furthest to the ***left*** of the group on the panel of the RTM when the board is in its normal operating orientation in the ATCA shelf. That is, the same order (top to bottom) as the front panel SFPs.

The LOS (**L**oss **O**f **S**ignal) field reads back the loss of signal indicator from each of SFP0 through SFP3 (bit 12: SFP0, 13:1, 14:2, 15:3). The LOS bit is set if the receiving optics of the given SFP fails to detect an optical signal.

The MOD_PRESENT lines are pulled up by resistors on the FLIC but pulled down by the SFP module when the module is inserted; thus 0 is “module present” and 1 is “module absent”.

The RATESEL bits are reserved for identification of multi-speed transceivers.

PROCESSOR FPGA: ADDRESS 0x105 : CCMUX_STATUS_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	FIFO_FULLs				FIFO_EMPTYs				EVENT_CNT_OVERFLOW				EVENT_CNT_UNDERFLOW			

The CCMUS status register provides four bit-fields indicative of the state of the four CCMUX FIFOs in the data processing pipeline. Each four-bit field presents the same bit of information for each of the four pipelines.

- The FIFO_FULL bits are set if the CCMUX FIFO goes full. This should never happen unless the FLIC pipeline is halted by a flow control condition and an excessively large event is sent by the SSB.
- The FIFO_EMPTY bits are set if the CCMUX FIFO goes empty. This state is often true.
- The EVENT_COUNT_OVERFLOW bit is set if an error causes the number of *events* within the FIFO to overflow the internal event counter. This should be impossible under normal operating circumstances.
- The EVENT_COUNT_UNDERFLOW bit is set if an error causes the number of *events* to count down below zero, indicative that the Data Merge machine had an error and took data where none was available.

PROCESSOR FPGA: ADDRESS 0x106 : SRAM_REFCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	SRAM Reference Clock rate in MHz															

The SRAM REFCLK counter provides a measurement of the *rate* at which the SRAM machine clock is running. The rate is expressed in MHz, and the rate should be 80.

PROCESSOR FPGA: ADDRESS 0x107 : DDR_REFCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	DDR Reference Clock rate in MHz															

The DDR REFCLK counter provides a measurement of the *rate* at which the DDR clock (used as the main pipeline processing clock) is running. The rate is expressed in MHz, and the rate should be 200.

PROCESSOR FPGA: ADDRESS 0x108 : GTX112_REFCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX112 Reference Clock rate in MHz															

The GTX REFCLK counter provides a measurement of the *rate* at which the SERDES reference clock (generated by the external clock chip controlled by FPGA U3) is running. The rate is expressed in MHz, and the rate is a function of the speed at which GTX112 is set to run. For normal 2Gbps operation this is 125MHz. In a 3Gbps setup, the speed would be 187.5MHz, which would read either 187 or 188.

PROCESSOR FPGA: ADDRESS 0x109 : GTX112_TXCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX 112 TX Clock rate in MHz															

The GTX TXCLK counter provides a measurement of the *rate* at which the SERDES transmitter-side word clock is running. The rate is expressed in MHz, and the rate is a function of the speed at which GTX112 is set to run. For normal 2Gbps operation this is 125MHz. In a 3Gbps setup, the speed would be 187.5MHz, which would read either 187 or 188.

PROCESSOR FPGA: ADDRESS 0x10A : GTX112_RXCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX 112 RX Clock rate in MHz															

The GTX RXCLK counter provides a measurement of the *rate* at which the SERDES receiver-side word clock is running. This is the word clock that is derived from the data stream The rate is expressed in MHz, and the rate is a function of the speed at which GTX112 is set to run. For normal 2Gbps operation this is 125MHz. In a 3Gbps setup, the speed would be 187.5MHz, which would read either 187 or 188.

PROCESSOR FPGA: ADDRESS 0x10B : GTX116_REFCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX116 Reference Clock rate in MHz															

The GTX REFCLK counter provides a measurement of the *rate* at which the SERDES reference clock (generated by the external clock chip controlled by FPGA U1) is running. The rate is expressed in MHz, and the rate is a function of the speed at which GTX111 is set to run. For normal 2Gbps operation this is 125MHz. In a 3Gbps setup, the speed would be 187.5MHz, which would read either 187 or 188.

PROCESSOR FPGA: ADDRESS 0x10C : GTX116_TXCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX 116 TX Clock rate in MHz															

The GTX TXCLK counter provides a measurement of the *rate* at which the SERDES transmitter-side word clock is running. The rate is expressed in MHz, and the rate is a function of the speed at which GTX116 is set to run. For normal 2Gbps operation this is 125MHz. In a 3Gbps setup, the speed would be 187.5MHz, which would read either 187 or 188.

PROCESSOR FPGA: ADDRESS 0x10D : GTX116_RXCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX 116 RX Clock rate in MHz															

The GTX RXCLK counter provides a measurement of the *rate* at which the SERDES receiver-side word clock is running. This is the word clock that is derived from the data stream The rate is expressed in MHz, and the rate is a function of the speed at which GTX116 is set to run. For normal 2Gbps operation this is 125MHz. In a 3Gbps setup, the speed would be 187.5MHz, which would read either 187 or 188.

PROCESSOR FPGA: ADDRESS 0x10E : Unused register

PROCESSOR FPGA: ADDRESS 0x10F : GTX116_RX_ERR_CNT_MUX

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX 116 RX Error Counter (multiplexed)															

This register provides access to the PRBS Frame Check error counter of all four SERDES links in GTX 116. When performing PRBS link checks, the Frame Check error counter counts how many data errors were found. Bits 9:8 of the ILA_MUX_CTL_REG found at address 0x00B selects which of the four SERDES lanes of GTX 116 has its RX error counter routed out to this register. This register is *only* valid for PRBS link testing and has no meaning when the pipeline is in normal operation.

PROCESSOR FPGA: ADDRESS 0x110 – 0x11E : MONITOR FIFOs

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Various monitoring data															

Eight MONITOR FIFO registers are located at addresses 0x110, 0x112, 0x114, 0x116, 0x118, 0x11A, 0x11C and 0x11E. Due to the way the PIC parallel bus interface works there is always an unintended excess read cycle at the address *after* the selected address. Normally this is harmless but in the case of FIFOs these excess read transactions must be protected against. The FLIC thus reserves all odd-numbered register addresses from 0x111 through 0x11F as “FIFO protection addresses” that may not be used.

The actual data read from the different MONITOR FIFOs is dependent upon the settings in the various MON_FIFO_CTRL registers located at addresses 0x017 through 0x01E. As of 20150806, the MONITOR FIFOs are assigned as follows:

- MON_FIFO 0 (address 0x110) monitors the output of the CCMUX FIFO (between Core Crate Receiver and Merge state machines).
- MON_FIFO 1 (address 0x112) monitors the output of the SRAM FIFO (between SRAM lookup and Merge state machines).
- MON_FIFO 2 monitors the output of the Merge state machine.
- MON_FIFO 3 monitors the output of the SLINK_PRIMITIVE state machine.
- MON_FIFOs 4 through 7 are currently undefined.

PROCESSOR FPGA: ADDRESS 200 : PULSED_CTL_REG_200

Controls GTX 112 front panel SFP links.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y3				GTX X0Y2				GTX X0Y1				GTX X0Y0			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX112_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX112_RXRESET_DONE occurring some time later.

PROCESSOR FPGA: ADDRESS 201 : PULSED_CTL_REG_201

Controls GTX 112.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	X	X	X	X	Enable Timing Tags				FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- Bits 11:8 set flip-flops in the GTX112 PRBS Frame Check logic that will cause the *next* event to have its 'ILA TAG' set in the various FIFOs. The 'ILA TAG' is intended to allow capture of the same event at all stages of processing using the internal Chipscope analyzers.

PROCESSOR FPGA: ADDRESS 202 : PULSED_CTL_REG_202

Reserved for controlling GTX 113 links. Mapping would be identical to Address 200.

PROCESSOR FPGA: ADDRESS 203 : PULSED_CTL_REG_203

Reserved for controlling GTX 113 features. Mapping would be similar to Address 201.

PROCESSOR FPGA: ADDRESS 204 : PULSED_CTL_REG_204

Reserved for controlling GTX 114 links. Mapping would be identical to Address 200.

PROCESSOR FPGA: ADDRESS 205 : PULSED_CTL_REG_205

Reserved for controlling GTX 114 features. Mapping would be similar to Address 201.

PROCESSOR FPGA: ADDRESS 206 : PULSED_CTL_REG_206

Reserved for controlling GTX 115 links. Mapping would be identical to Address 200.

PROCESSOR FPGA: ADDRESS 207 : PULSED_CTL_REG_207

Reserved for controlling GTX 115 features. Mapping would be similar to Address 201.

PROCESSOR FPGA: ADDRESS 208 : PULSED_CTL_REG_208

Controls GTX116 (RTM)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y19				GTX X0Y18				GTX X0Y17				GTX X0Y16			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX116_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX116_RXRESET_DONE occurring some time later.

PROCESSOR FPGA: ADDRESS 209 : PULSED_CTL_REG_209

Controls GTX116 (RTM)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	X	X	X	X	User Reset Request				FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- Bits 11:8 are reset requests to the SLINK_RESET_CONTROLLER machines in GTX116. These resets combine with the SLINK Reset Controller GO bits in the SLINK_CTL register to determine what the reset state machine will do. Pulsing these bits should restart the reset sequence to an initial IDLE state, but then the GO bit has to be turned on to make the machine proceed from there.

PROCESSOR FPGA: ADDRESS 20A,20B : UNUSED

DEFAULT VALUE AT POWER-UP : 0x0000.

PROCESSOR FPGA: ADDRESS 20C : PULSED_CTL_REG_20C

Resets to Monitor FIFOs.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO	X	X	X	X	X	X	X	X	MF7 RST	MF6 RST	MF5 RST	MF4 RST	MF3 RST	MF2 RST	MF1 RST	MF0 RST

BIT DEFINITIONS

- Each of the MFx RST bits resets the associated Monitor FIFO, clearing the FIFO.
- After reset each FIFO automatically refills with new data based upon its design settings, thus writing the reset acts as an asynchronous data capture. The various Monitor FIFOs are currently set to monitor the following points in the data pipeline:
    - Monitor FIFO 0 collects the data falling out of the CCMUX FIFO, with the write enable of the Monitor FIFO set equal to the read enable of the CCMUX FIFO. MON_FIFO_CTL_REG(0) may be used to select which pipeline is monitored.
    - Monitor FIFO 1 collects the data falling out of the SRAM FIFO, with the write enable of the Monitor FIFO set equal to the read enable of the SRAM FIFO. MON_FIFO_CTL_REG(1) may be used to select which pipeline is monitored.

- Monitor FIFO 3 collects the data falling out of the MERGE FIFO, with the write enable of the Monitor FIFO set equal to the read enable of the MERGE FIFO. MON_FIFO_CTL_REG(2) may be used to select which pipeline is monitored.
- Monitor FIFO 0 collects the data being written to the RTM FIFO, with the write enable of the Monitor FIFO set equal to the write enable of the RTM FIFO. MON_FIFO_CTL_REG(3) may be used to select which pipeline is monitored.

PROCESSOR FPGA: ADDRESSES 0x20D and 0x20E : UNUSED

DEFAULT VALUE AT POWER-UP : 0x0000.

PROCESSOR FPGA: ADDRESS 20E : PULSED_CTL_REG_20E

General purpose control.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO	CLKGEN RESET	X	X	X	X	X	X	X	X	X	X	X	CNTR RST 3	CNTR RST 2	CNTR RST 1	CNTR RST 0

BIT DEFINITIONS

- Bit 15 (CLKGEN RESET), forces a reset of the external SLINK (GTX 116) reference clock generator chip (***U1 ONLY***).
- The four CNTR RST bits will cause all pipeline diagnostic counters for a given pipeline to be reset.

PROCESSOR FPGA: ADDRESS 20F : SUBSECTION_PULSED_RESETS_REG

General purpose pulsed control register, specifically aimed at resets. This register is a pulsed version of address 0x01F.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO	G116 FREAD	G116 FIFO	SLINK PRIM	MERGE	Hola Core	TLK	SRAM B	SRAM A	CCMUX FIFO resets				Core Crate Rcvr Resets			

BIT DEFINITIONS

- Bits 3:0 are pulsed resets for four Core Crate Rcvr blocks. The DDR-domain ILA monitors these bits as ILA bit 88 (section selected by ILA mux controls).
- Bits 7:4 are pulsed resets for the four CCMUX FIFOs.
- Bit 8 resets SRAM machine A; bit 9 resets SRAM machine B.
- Bit 10 resets the TLK reformatter logic from CERN in all four GTX116 copies.
- Bit 11 resets the Hola Core (S-link) logic taken from CERN in all four GTX116 copies.
- Bit 12 resets all Merge state machines and all Merge FIFOs.
- Bit 13 resets all SLINK_PRIMITIVE machines.
- Bit 14 resets all GTX 116 event FIFOs.
- Bit 15 resets all GTX 116 FIFO reader machines.

Pass-through access to U1's external SRAM

Accesses to U1 with addresses in the range 0x10000 – 0x4FFFF will be treated as pass-through accesses to the external SRAM chips. U1 has four SRAMs (U156, U157, U159, U158) connected in two pairs. U156 and U157 are collectively referred to as "LUT1"; chips at U158/U159 are "LUT2". The two "LUTx" groups share address and data buses but have separated OE, WE and CE controls. The mapping is as follows:

- Addresses 0x10000 – 0x1FFFF provide access to U156.
- Addresses 0x20000 – 0x2FFFF provide access to U157.
- Addresses 0x30000 – 0x3FFFF provide access to U159.
- Addresses 0x40000 – 0x4FFFF provide access to U158.

Each SRAM has a 21-bit address range, larger than the window provided. The upper five bits of the address provided to the SRAM come from address extension registers, located at addresses 0x0300, 0x0301, 0x0302 and 0x0303 respectively. This provides a moveable 64K address window per SRAM, matching the 64K address space of the PIC processor.

SSB Emulation Build of FPGA U2

SSB EMULATOR U2 : ADDRESS 000 : CLOCK_CONTROL_REG

FPGA U2 does not control any clock generators. The Clock Control register of U2 exists but has no function.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Unused, writable, has no effect															

DEFAULT VALUE AT POWER-UP : 0x0000.

SSB EMULATOR U2 : ADDRESS 001 : LED_REG

Generic diagnostic register allowing the user to play with two of the board's front panel LEDs.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	X	X	LED7	LED6

DEFAULT VALUE AT POWER-UP : 0x0000.

SSB EMULATOR U2 : ADDRESS 002 : GENERAL_CTL_REG

Generic control register provided to allow the user a way to override automatic settings.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	RST SRC	G116 FGRST	G116 FCRST	X	X	G115 FGRST	G115 FCRST	G114 FGRST	G114 FCRST	G112 FGRST	G112 FCRST	X	G113 FGRST	G113 FCRST	X	X

NOTE TO THE USER:

The format and usage of the GENERAL_CTL_REG in the Emulator build differs quite a bit from that found in the pipeline processor ("U1") build.

BIT DESCRIPTIONS

- Bit 15, if clear, means that the RTX and RRX bits of this register are manual resets to the frame generator (TX) and frame checker (RX) blocks for the GTX blocks. If bit 15 is set, the resets for these units are derived from control signals from the SERDES cores.
    - Bits 14:13 are the manual frame generator and frame checker resets, respectively, for GTX 116.
    - Bits 10:9 are the manual frame generator and frame checker resets, respectively, for GTX 115.
    - Bits 8:7 are the manual frame generator and frame checker resets, respectively, for GTX 114.
    - Bits 6:5 are the manual frame generator and frame checker resets, respectively, for GTX 112.
    - Bits 3:2 are the manual frame generator and frame checker resets, respectively, for GTX 113.

DEFAULT VALUE AT POWER-UP: 0x0000.

U2 Data Emulation notes (from 2014 – danger, these may be out of date!)

The GTX 112 implementation for FPGA U2 in the prototype module implements a data emulator rather than the normal GTX 112 that receives and processes SSB data. The data emulator generates SSB records for loopback testing. This data emulation module has multiple modes of operation:

1. The default (reset) state is to send comma characters all the time.
2. If the user sets any of bits 11:8 of PULSED_CTRL_REG_201, the indexed SERDES link of GTX112 will dump the contents of the user-filled FIFO, then return to sending commas all the time.
3. If the user sets any of bits 15:12 of PULSED_CTRL_REG_201, the indexed SERDES link of GTX112 will send emulated SSB data, amount controlled by the NUMBER_OF_RECORDS (addresses 0x14 – 0x17), RECORD_DELAY_CTRL (addresses 0x18 – 0x1B) and NUMBER_OF_TRACKS (addresses 0x20-0x23) registers. Upon completion of the data as requested, the machine returns to sending comma characters.
    a. The user may set any of bits 11:8 of the CORE_CRATE_CONTROL_REG (address 0x01F), indexed per SERDES link of GTX112, prior to starting the transmission of SSB data. Setting these bits will cause the SSB emulation to recycle and re-start after all the data specified by the NUMBER_OF_RECORDS and NUMBER_OF_TRACKS settings, and repeat the process, thus looping interminably until either this "send forever" bit is cleared or the machine is reset.
4. If the user sets any of bits 3:0 of the CORE_CRATE_CONTROL_REG, the indexed SERDES link of GTX 112 enters PRBS mode, sending a pseudo-random testing sequence controlled by the PRBS_CONTROL registers (addresses 0x05 through 0x08) and the TX_SEED registers (addresses 0x0C through 0x0F).

Procedure to send FIFO data

1. Ensure the SERDES links (sender and receiver) are locked. Reset as required.
2. Load the user data FIFO at address 0x80, 0x81, 0x82 or 0x83 (one address per SERDES, 0-3, in order) with the desired data.
3. Set the required bits (11:8) in the PULSED_CTRL_REG at address 0x0201 (bit 11: SERDES 3; bit 10: SERDES 2; bit 9: SERDES 1; bit 8: SERDES 0) to send the FIFO data.

Procedure to send SSB data

A. Reset the clock generator chips as controlled by both U1 and U3.
    a. Write the appropriate clock speed code to U1, address 0 (SLINK_CLOCK_CONTROL register). Normal value is either 1 (2Gbps) or 3 (3Gbps).
    b. Write 0x1 to address 0x20E of U1 (PULSED_CTL_REG_20E) to force a reset of the clock chip.
    c. Write the appropriate clock speed code to U3, address 0 (SFP_CLOCK_CONTROL register). Normal value is either 1 (2Gbps) or 3 (3Gbps).
    d. Write 0x1 to address 0x200 of U1 (PULSED_CTL_REG_20E) to force a reset of the clock chip.

B. Force a transmitter reset to all RTM links and front panel SFP links to insure that the transmitters are re-locked onto the new clock frequency
    a. Write 0x1111 to address 0x208 of FPGA U1.
    b. Write 0x1111 to address 0x200 of FPGA U1.
    c. Write 0x1111 to address 0x208 of FPGA U2.
    d. Write 0x1111 to address 0x200 of FPGA U2.

C.

// Set up U2 to be sending PRBS data via SERDES link 0 to U1, SERDES link 3.

// Set U1, GTX112, ILA mux to monitor SERDES link 3.
// Set U1, GTX116, ILA mux to monitor SERDES link 3.
// Set U1, DDR domain ILA mux, to monitor channel 3.
SendWrite(targetFpgaU1,0x0000000B, 0x0F03);
// Set U2, GTX112, ILA mux to monitor SERDES link 0.
// Set U2, GTX116, ILA mux to monitor SERDES link 0.
SendWrite(targetFpgaU2,0x0000000B, 0x0000);

// Set U1 and U2 to use manual control for resetting GTX links.
// this write to the General Control Register also turns off the Core Crate Receiver and Merge machines.
// this value also clears the SRAM Access bit, so access to the SRAM is through the register I/O.
// we will do SendSets to turn things on later.
SendWrite(targetFpgaU1,0x00000002, 0x0000);
SendWrite(targetFpgaU2,0x00000002, 0x0000);

// Put frame generator and frame checker state machines into reset in both U1 and U2.
SendSet(targetFpgaU1,0x00000002, 0x6030);
SendSet(targetFpgaU2,0x00000002, 0x6030);

// With state machines in reset, whack GTX112 in both U1 and U2
SendWrite(targetFpgaU1,0x00000200, 0x1111);
SendWrite(targetFpgaU2,0x00000200, 0x1111);

// Release frame generator and frame checker state machine resets in both U1 and U2.
SendClear(targetFpgaU1,0x00000002, 0x6030);
SendClear(targetFpgaU2,0x00000002, 0x6030);

// turn on SFP transmitters in both U1 and U2
SendWrite(targetFpgaU1,0x00000004, 0x0000);
SendWrite(targetFpgaU2,0x00000004, 0x0000);

// At this point U1 should be sending PRBS to U2 over the front SFP. U2 should be sending commas to U1 over the front SFP.
// At this point U1 is also sending PRBS out the RTM over the SLINK SFPs. This should be changed to SLINK format for all links.

```
SendSet(targetFpgaU1,0x00000003, 0x00F0);

// Now we do step 6 of the handwritten script.
// Set SRAM access to state machine (bit 3 of GENERAL_CONTROL clear) in U1 (should already
be so)
// Enable Core Crate receiver machines (set bit 1 of GENERAL_CONTROL) in U1
// Enable data merge machines (set bit 4 of GENERAL_CONTROL) in U1
SendSet(targetFpgaU1,0x00000002, 0x0012);     //sets bits 4 and 1.

//Hit all Subsection Resets in U1, in order
SendWrite(targetFpgaU1,0x0000020F, 0x8000); //reset the GTX116 FIFO reader
SendWrite(targetFpgaU1,0x0000020F, 0x4000); //reset the GTX116 data FIFO
SendWrite(targetFpgaU1,0x0000020F, 0x2000); //reset the SLINK primitives
SendWrite(targetFpgaU1,0x0000020F, 0x1000); //reset the merge machines
SendWrite(targetFpgaU1,0x0000020F, 0x0300); //reset the SRAM machines
SendWrite(targetFpgaU1,0x0000020F, 0x00F0); //reset the CCMUX logic
SendWrite(targetFpgaU1,0x0000020F, 0x000F); //reset the core crate receivers

SendWrite(targetFpgaU1,0x0000020F, 0x0400); //reset the GTX116 TLK wrappers
SendWrite(targetFpgaU1,0x0000020F, 0x0800); //reset the GTX116 hola core logic

// now enable the SLINK reset state machine to go
SendClear(targetFpgaU1,0x00000003, 0x0F00);  //clear the GO bits to the reset machines
SendWrite(targetFpgaU1,0x00000209, 0x0F00); //request the reset machines to re-arm
SendSet(targetFpgaU1,0x00000003, 0x0F00);     //set the GO bits to the reset machines



//Set all ILA tag bits in U1, GTX 112
SendWrite(targetFpgaU1,0x00000201, 0x0F00);

//Now switch SRAM control back to state machine by setting bit 3 of GENERAL_CONTROL
register
SendSet(targetFpgaU1,0x00000002, 0x0008);     //set bit 3

//set the SSB emulator in U2 to have status words of 0xDDDD and 0xEEEE
SendWrite(targetFpgaU2,0x0000001D, 0xDDDD);
SendWrite(targetFpgaU2,0x0000001E, 0xEEEE);

//as last steps, set the FLIC status words in U1 to 0x1515 and 0x1616, respectively
SendWrite(targetFpgaU1,0x00000015, 0x1515);
SendWrite(targetFpgaU1,0x00000016, 0x1616);
```

1. Ensure the SERDES links (sender and receiver) are locked. Reset as required.
2. Load the NUMBER_OF_RECORDS, NUMBER_OF_TRACKS, TX_SEED and RECORD_DELAY_CTRL registers with the appropriate setup data.

3. Note that applying a reset to the entire TX chain by setting any of bits 0,2,4 or 6 of the PULSED_CTRL_REG at address 0x0201 will have the effect of resetting the USER_RUN_NUMBER and USER_LEVEL_1_ID values to zero. Otherwise, these automatically count, both increasing by 1 with each record transmitted.
4. Set bits 11:8 of the CORE_CRATE_CONTROL_REG as desired to enable or disable the "send forever" mode.
5. Set bits 15:12 of PULSED_CTRL_REG_201 to start the data generation.

Procedure to send PRBS data

1. Ensure the SERDES links (sender and receiver) are locked. Reset as required.
2. Hold the PRBS data generator reset by setting the appropriate bits within bits 3:0 of the CORE_CRATE_CONTROL_REG.
3. Load the PRBS_CONTROL registers with the desired configuration:
    a. Load PRBS_CONTROL(0) at address 0x005 with the number of commas to send before sending the PRBS pattern.
    b. Load PRBS_CONTROL(1) at address 0x006 with the number of PRBS words to send before inserting a block of commas.
    c. Load PRBS_CONTROL(2) at address 0x007 with the number of commas to send in each block of commas inserted into the data stream. Only bits 3:0 matter.
    d. Load PRBS_CONTROL(3) at address 0x008 with the total number of PRBS words to send, exclusive of inserted commas, before restarting the PRBS block.
    e. The sender and receiver devices must be loaded with identical parameters or the data checking in the receiver will fail.
4. Configure the receiver FPGA's GTX to match the PRBS_CONTROL settings of the sender FPGA. Reset and then release the receiver logic.
5. Enable the sending of PRBS data by setting the appropriate bits within bits 7:4 of the CORE_CRATE_CONTROL _REG.
6. Release the PRBS machine from reset by clearing the appropriate bits (3:0) in the CORE_CRATE_CONTROL_REG.
7. Data will be sent until the enable bits of step (5) are cleared.

SSB EMULATOR U2 : ADDRESS 003 : SLINK_CTL_REG

Reserved for future misuse; generally will control the TDIS pins of the rear transition module.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	ENBL TIM TAGS	RST ERR CNT	X	X	X	X	X	X	X	X	X	X	RTM TDIS			

BIT DESCRIPTIONS

- Bit 15, if set, enables the FRAME_CHECK machine within GTX116 (RTM) to insert ILA timing tags, used for diagnostics.
- Bit 14, if set, resets the GTX116 FRAME_CHECK machine's PRBS error counter to zero.
- Bits 3:0 directly drive the TDIS lines of the four SFP modules of the rear transition module driven by the FPGA. Each bit, if ***set***, will ***disable*** the SFP unit.

DEFAULT VALUE AT POWER-UP : 0x0000.

SSB EMULATOR U2 : ADDRESS 004 : SFP_CTL_REG

Enables/disables the SFP fiber interfaces on the front panel.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	ENBL TIM TAGS	RST ERR CNT	X	X	X	X	X	X	X	X	X	X	TDIS3	TDSI2	TDIS1	TDIS0

BIT DEFINITIONS

- Bit 15, if set, enables the FRAME_CHECK machine within GTX112 (front panel SFPs) to insert ILA timing tags, used for diagnostics.
- Bit 14, if set, resets the GTX 112 FRAME_CHECK machine's PRBS error counter to zero.
- Bits 3:0 directly drive the TDIS lines of the four SFP modules on the front panel of the FLIC driven by the FPGA. Each bit, if ***set***, will ***disable*** the SFP unit.

DEFAULT VALUE AT POWER-UP : 0x0000.

SSB EMULATOR U2 : ADDRESS 005 - 008 : PRBS CONTROL REGISTERS

This set of four registers defines the (Pseudo-Random Bit Sequence) PRBS control parameters of the FRAME_GEN machines in ***both GTX112 and GTX116***. A PRBS generator is available to drive a programmable data sequence out any SERDES link. A matching PRBS receiver will lock on to the pattern and compare received data to transmitted data for bit-error-rate-testing (BERT).

REGISTER 0x0005: NUMBER OF COMMAS AFTER RESET

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	INITIAL NUMBER OF COMMAS AFTER RESET															

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0020.

REGISTER 0x0006: NUMBER OF WORDS TO SEND BEFORE INSERTING COMMA(S)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Number of words to send before inserting comma character(s)															

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0040.

REGISTER 0x0007: NUMBER OF COMMAS TO SEND IN COMMA BREAKS

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	UNUSED												# of commas			

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0002.

REGISTER 0x0008: TOTAL NON-COMMA PATTERN LENGTH BEFORE PATTERN RESTART

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Number of words to send before restarting PRBS sequence.															

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0100.

General notes on pseudo-random sequence

The pseudo-random sequence is generated using a shift register with exclusive-or gates. In the current version of the U2 code, four PRBS generators and four PRBS receivers are connected to the four SERDES units associated with the four front panel SFP connections. The seed values for each PRBS are different, stored in registers at addresses 0x000C, 0x000D, 0x000E and 0x000F. The default seeds are 0x0135, 0x1234, 0x5678 and 0xF18A. A PRBS spreadsheet in the code repository may be used to generate the expected data stream for any seed.

The PRBS machines FRAME_GEN and FRAME_CHECK are not the machines generated in the example design by the Xilinx Coregen tools. They have been written specifically for the FLIC. The FRAME_GEN machine starts by sending an initial number of comma characters defined by PRBS_CONTROL(0). The machine then sends a block of exactly three words of value 0x0000, followed by a number of PRBS words. The receiving FRAME_GEN machine looks for the three words of 0x0000 (a unique value as a properly seeded PRBS will not generate 0x0000) as a starting condition for its own, separate PRBS. The first non-zero data value received after the block of three zeroes is the *seed* value that is loaded into the FRAME_CHECK machines PRBS. For all non-comma words after the seed value, the receiver's PRBS is compared against the data sent by the transmitter and all mismatches are flagged and counted.

During the transmission of PRBS data comma characters are inserted every so often, as controlled by PRBS_CONTROL(1). The number of comma characters sent in these comma breaks is set in PRBS_CONTROL(2). An overall total data word count is kept, and then the count matches the value in PRBS_CONTROL(3) a new block of three zeroes is sent to re-seed the receiver's PRBS. The purpose of the FRAME_GEN and FRAME_CHECK machines is to provide a direct method of measuring the bit error rate of the fiber links of the FLIC.

General notes on core crate emulation

The data for the core crate emulator contains a couple of counted values, a couple of user-defined values, and then a bunch of track data. The same pseudo-random number generator described above is used for all the track data.

SSB EMULATOR U2 : ADDRESS 009 : UNUSED

DEFAULT VALUE AT POWER-UP : 0x0000.

SSB EMULATOR U2 : ADDRESS 00A : UNUSED

DEFAULT VALUE AT POWER-UP : 0x0000.

SSB EMULATOR U2 : ADDRESS 00B : ILA_MUX_CTL_REG

Controls operation of the multiplexed latch in the GTX instantiations preceding the ILA for the GTX quad.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	DDR MUX SEL		GTX 116 MUX SEL		GTX 115 MUX SEL		GTX 114 MUX SEL		GTX 113 MUX SEL		GTX 112 MUX SEL	

BIT DEFINITIONS

- The GTX MUX SEL bits select which of the four SERDES links in the GTX quad is sampled for the GTX ILA. The order and format of the ILA doesn't change, just which SERDES is being monitored.
    - For GTX 112, 00:X0Y0, 01:X0Y1, 10:X0Y2, 11:X0Y3. Same relative order for other GTX quads.
- The DDR MUX SEL bits select which core crate receiver machine is sampled for the DDR ILA.

DEFAULT VALUE AT POWER-UP : 0x0000.

SSB EMULATOR U2 : ADDRESSES 00C, 00D, 00E, 00F : TX_SEED REGISTERS

These registers define the starting (seed) value to use in the PRBS generators (frame generators). The register at address 0x00C defines the seed for link 0 of GTX112 and also for link 0 of GTX116. TX_SEED0 defaults at power-up to 0x0135; TX_SEED1 to 0x1234, TX_SEED2 to 0x5678 and TX_SEED3 to 0xF18A.

SSB EMULATOR U2 : ADDRESSES 010, 011, 012, 013 : FIFO PROG THRESHOLDS

Registers 0x0010 and 0x0011 define the Programmable Empty and Programmable Full thresholds of the SFP input FIFOs. Similarly, registers 0x0012 and 0x0013 define the Programmable Empty and Programmable Full for the RTM output FIFOs.

SSB EMULATOR U2 : ADDRESSES 014, 015, 016, 017 : NUMBER OF RECORDS REGISTERS

These registers control the operation of the Core Crate Emulator logic in the U2 firmware. There are four registers, one per SERDES link in the Quad. The GTX112 Quad and the GTX116 Quad are both tied to these registers so that link #n of GTX112 will be set the same as link #n of GTX116.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	NUMBER OF RECORDS TO SEND															

The sixteen-bit value written to these records is loaded into a counter to determine the number of records that is sent in response to enabling the emulator logic.

SSB EMULATOR U2 : ADDRESSES 018, 019, 01A, 01B : RECORD DELAY REGISTERS

These registers control the operation of the Core Crate Emulator logic in the U2 firmware. There are four registers, one per SERDES link in the Quad. The GTX112 Quad and the GTX116 Quad are both tied to these registers so that link #n of GTX112 will be set the same as link #n of GTX116.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	FIX/ RND	RAND RANGE			FIXED # of RECORDS											

BIT DESCRIPTIONS

- Bit 15 selects whether the number of tracks will be fixed (bit SET) or pseudo-random (bit CLEAR).
    - In the FIXED mode (bit 15 set), the number of tracks is determined by the value of bits 11:0 and bits 14:12 are ignored.
    - In the RANDOM mode (bit 15 clear), the number of tracks generated each event is a bounded pseudo-random number, selected by the RAND RANGE (bits 14:12) and FIXED # OF TRACKS (bits 11:0) fields.
        - The RAND RANGE field selects one of eight ranges:
        - If bits 14:12 are “000”, the random mode degrades to a fixed number of tracks, defined by the FIXED # OF TRACKS.

- Settings from “001” through “111” select a power-of-two range of a random value that is added to the FIXED # OF TRACKS value so that the number of tracks will range as follows.
- “001” : Either FIXED # OF TRACKS or (FIXED # OF TRACKS + 1)
- “010” : between FIXED # OF TRACKS and (FIXED # OF TRACKS + 3)
- “011” : between FIXED # OF TRACKS and (FIXED # OF TRACKS + 7)
- “100” : between FIXED # OF TRACKS and (FIXED # OF TRACKS + 15)
- “101” : between FIXED # OF TRACKS and (FIXED # OF TRACKS + 31)
- “110” : between FIXED # OF TRACKS and (FIXED # OF TRACKS + 63)
- “111” : between FIXED # OF TRACKS and (FIXED # OF TRACKS + 127)

SSB EMULATOR U2 : ADDRESS 01C : MONITOR FIFO CONTROL REGISTER

This register controls the operation of the GTX112 Monitor FIFO buffer, whose data is available at address 0x010F (GTX112_MONITOR_FIFO_DOUT).

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW															LINK SEL	

BIT DEFINITIONS
The LINK_SEL bits select which of the four SFP links (0-3) in the GTX112 Quad is monitored.
As of 20150804 the Monitor FIFO function is not implemented in U2 and writes to this register have no effect.

SSB EMULATOR U2 : ADDRESS 01D : CORE_CRATE_STATUS_REG

Defines the data value that is sent by the Core Crate Emulation logic for the Status word.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	CORE CRATE STATUS VALUE															

DEFAULT VALUE AT POWER-UP : 0x0000.

SSB EMULATOR U2 : ADDRESS 01E : CORE_CRATE_ERROR_REG

Defines the data value that is sent by the Core Crate Emulation logic for the Error word.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	CORE CRATE ERROR VALUE															

DEFAULT VALUE AT POWER-UP : 0x0000.

SSB EMULATOR U2 : ADDRESS 01F : CORE_CRATE_CONTROL_REG

This register controls the operation of the Core Crate Emulator logic in the U2 firmware.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SEND LONG L1ID				SEND FOREVER				RESET PRBS MACHINE				ENABLE PRBS DATA			

BIT DESCRIPTIONS

- Bits 3:0 enable the CoreCrateEmulator logic block within GTX 112 to send the PRBS data from the JTA_FRAME_GEN logic block out the front panel SFP links, for BER testing. Each bit is associated with one of the four SFP links of GTX 112 (0 to 0, 1 to 1, etc.).
- Bits 7:4, in the same SERDES order as bits 3:0, hold the JTA_FRAME_GEN logic in reset when set.
- Bits 11:8, in the same SERDES order as bits 3:0, tell the CoreCrateEmulator logic to run forever when "SSB" data is being transmitted. Normally, when "SSB" data is sent, one block of records as controlled by the NUMBER_OF_RECORDS registers is sent. When these "send forever" bits are set, the NUMBER_OF_RECORDS is ignored and data runs forever.
    - Upon clearing these "send forever" bits, the sending of data will stop after no more than the NUMBER_OF_RECORDS of additional records are sent. The "send forever" bit simply causes the internal record counter to be reset back to NUMBER_OF_RECORDS after the internal record counter counts down to zero, the normal stop condition. Clearing these control bits will cause normal cessation of data and a return to the idle state the next time the internal counter hits zero.
- Bits 15:12 select whether the Emulator logic will send short (24-bit) or long (32 bit) Level 1 ID values.
    - If the SEND LONG L1 ID bit is *CLEAR*, the emulator sends bits 23:0 of the internally calculated USER_LEVEL_1_ID value and bits 31:24 of the Level 1 ID field are all zeroes.
    - If the SEND LONG L1 ID bit is *SET*, the emulator sends one of two long formats dependent upon the state of bit 0 of the CORE CRATE AUX CTL register at address 02D:
        - If bit 0 of the CORE CRATE AUX CTL register is *SET*, then the full 32-bit USER COUNTER value is used as the Level 1 ID.
        - If bit 0 of the CORE CRATE AUX CTL register is *CLEAR*, then the 24-bit Level 1 ID value is concatenated with an 8-bit EVENT COUNTER to form the 32-bit Level 1 ID.
    - The EVENT COUNTER is sensitive to the RESET_SSB_COUNTERS signal that comes from a pulsed control register. The EVENT COUNTER's response to RESET_SSB_COUNTERS is also modulated by the SEND LONG L1 ID bit:
        - If the SEND LONG L1 ID bit is *CLEAR*, the Event Counter is reset to 0x01 by RESET_SSB_COUNTERS.
        - If the SEND LONG L1 ID bit is *SET*, the Event Counter is *incremented* by RESET_SSB_COUNTERS.
        - RESET_SSB_COUNTERS also has the effect of resetting the USER LEVEL 1 ID value to zero.

SSB EMULATOR U2 : ADDRESSES 020 - 023 : NUMBER_OF_TRACKS

These registers control the operation of the Core Crate Emulator logic in the U2 firmware. There are four registers, one per SERDES link in the Quad. The GTX112 Quad and the GTX116 Quad are both tied to these registers so that link #n of GTX112 will be set the same as link #n of GTX116.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	FIX/ RND	RAND RANGE			RAND OFFSET				FIXED # of TRACKS							

BIT DESCRIPTIONS

- Bit 15 selects whether the number of tracks will be fixed (bit SET) or pseudo-random (bit CLEAR).
    - In the FIXED mode (bit 15 set), the number of tracks is determined by the value of bits 7:0 and bits 14:8 are ignored.
    - In the RANDOM mode (bit 15 clear), the number of tracks generated each event is a bounded pseudo-random number, selected by the RAND RANGE (bits 14:12) and RAND OFFSET (bits 11:8) fields.
        - The RAND RANGE field selects one of eight ranges:
        - If bits 14:12 are “000”, the random mode degrades to a fixed number of tracks, defined by the RAND OFFSET.
        - Settings from “001” through “111” select a power-of-two range of a random value that is added to the RAND OFFSET value so that the number of tracks will range as follows.
        - “001” : Either RAND OFFSET or (RAND OFFSET + 1)
        - “010” : between RAND OFFSET and (RAND OFFSET + 3)
        - “011” : between RAND OFFSET and (RAND OFFSET + 7)
        - “100” : between RAND OFFSET and (RAND OFFSET + 15)
        - “101” : between RAND OFFSET and (RAND OFFSET + 31)
        - “110” : between RAND OFFSET and (RAND OFFSET + 63)
        - “111” : between RAND OFFSET and (RAND OFFSET + 127)

SSB EMULATOR U2 : ADDRESS 024/025/026 : GTX113/114/115_CTL_REG

These registers control the operation of the Generic_GTX block used to implement inter-FGPA serial links.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Unused								ENABLE TIMING TAGS				ENABLE FIFO DATA			

BIT DESCRIPTIONS

- Bits 3:0 control the TX multiplexer logic within each GTX block. Each bit is associated with one of the four SERDES links of the GTX Quad.
    - If the bit is *SET*, the data transmitted by the SERDES is the data available from a TX FIFO. A state machine constantly monitors the TX FIFO and when a full event is available, the TX machine reads the entire event out.
    - If the bit is *CLEAR*, the data transmitted by the SERDES is PRBS test data generated by the *frame generator* logic.
- Bits 7:4, in the same SERDES order as bits 3:0, enable the automatic insertion of "timing tags" into the received data stream.
    - If the bit is *SET*, the "timing tag" (an extra FIFO bit not part of the data) is set each time the incoming data is either X"0000" or X"5A5A". A different "timing tag" bit is set for each of the two data values.
    - These two "timing tag" bits are connected to the Chipscope RX-side of the Generic_GTX logic and may be used to easily trigger the capture of received data.
    - A value of X"0000" marks the start of a PRBS data pattern. A value of X"5A5A" is one of the values used in the Record Trailer of SSB data for synchronization.

SSB EMULATOR U2 : ADDRESS 027 – 02C : GTX113/114/115 FIFO THRESHOLDS (RESERVED)

Controls GTX113, GTX114 and GTX115 (Inter-FPGA links)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	FIFO Programmable threshold															

These currently non-functional register addresses are reserved for the future implementation of programmable FULL and programmable EMPTY thresholds in the RX-side FIFOs of inter-FPGA links.

SSB EMULATOR U2 : ADDRESS 02D : CORE_CRATE_AUX_CTL

Controls GTX112 (SFP) and GTX116 (RTM)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	X	X	X	X	X	X	X	X	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.

SSB EMULATOR U2 : ADDRESS 02E : COUNTER_CTL

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	GTX 113		GTX 114		GTX 115		NA	NA	NA	NA	NA	NA
RW	X	X	X	X	CNT RESET	CNT MODE	CNT RESET	CNT MODE	CNT RESET	CNT MODE	X	X	X	X	X	X

BIT DEFINITIONS

- CNT RESET bits hold the various counters (REFCLK, TXCLK, RXCLK) inside the Generic_GTX block reset.
- CNT MODE bits set the various counters inside a Generic_GTX block into RATE mode (bit SET) or COUNT mode (bit CLEAR).

SSB EMULATOR U2 : ADDRESS 02F/20F : HELD_RESETS / PULSED_RESETS

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
RW	X	X	TX MACH RST	X	X	X	TX FIFO RST	X	X	X	X	X	X	X	X	X

BIT DEFINITIONS

The value of the HELD_RESETS register is bit-by-bit ORed with the value written to the PULSED_RESETS register to create the SUBSECTION_RESETS bit vector within the code. The intent (only partially realized as of August 4, 2015) is to provide a mechanism akin to that previously implemented for GTX112 and GTX116 implementations in which the user may either hold reset or momentarily reset various Generic_GTX functions. The intention was to provide four bits per GTX block:

- TX FIFO reset
- TX machine reset
- RX FIFO reset
- RX machine reset

However, this has not been realized. As of the current writing (8/4/15) only bits 9 and 13 do anything. Bit 9 is the TX FIFO reset that applies to all of GTX113, GTX114 and GTX115 identically, and bit 13 is a TX machine reset that applies to all of GTX113, GTX114 and GTX115.

Future revisions of the code will revisit these registers.

SSB EMULATOR U2: ADDRESS 100 : CODE_REVISION

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Major Revision				Minor Revision				Sub-Revision				Day Index			

The CODE_REVISION register provides a location to read the current version of the FLIC firmware. This register is changed when the firmware is modified to allow the user to determine if the board contains the latest revision of firmware. The current value as of November 6, 2014 is 0x0105 (Version 0.1.0.5).

SSB EMULATOR U2: ADDRESS 101 : CODE_DATE_YYYY

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Year of last code revision															

The CODE_DATE_YYYY register provides a location to read the date, as stored by the firmware engineer, of the version of code within the FPGA.

SSB EMULATOR U2: ADDRESS 101 : CODE_DATE_MMDD

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Month of last code revision								Day of month of last code revision							

The CODE_DATE_MMDD register provides a location to read the date, as stored by the firmware engineer, of the version of code within the FPGA.

SSB EMULATOR U2 : ADDRESS 103 : SFP_STATUS_REG

Reserved for future misuse; generally will control the TDIS pins of the rear transition module.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	LOS				MOD_PRESENT				RATESEL				TFAULT			

The LOS (**L**oss **O**f **S**ignal) field reads back the loss of signal indicator from each of SFP0 through SFP3 (bit 12: SFP0, 13:1, 14:2, 15:3). The LOS bit is set if the receiving optics of the given SFP fails to detect an optical signal.

The MOD_PRESENT lines are pulled up by resistors on the FLIC but pulled down by the SFP module when the module is inserted; thus 0 is “module present” and 1 is “module absent”.

The RATESEL bits are reserved for identification of multi-speed transceivers.

The TFAULT bits, if high, indicate a transmitter fault. TFAULT is an open-collector signal requiring a pullup resistor on the FLIC to operate.

SSB EMULATOR U2 : ADDRESS 104 : RTM_SFP_STATUS_REG

Reserved for future misuse; generally will control the TDIS pins of the rear transition module.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	LOS				MOD_PRESENT				RATESEL				0	0	0	0

The LOS (**L**oss **O**f **S**ignal) field reads back the loss of signal indicator from each of SFP0 through SFP3 (bit 12: SFP0, 13:1, 14:2, 15:3). The LOS bit is set if the receiving optics of the given SFP fails to detect an optical signal.

The MOD_PRESENT lines are pulled up by resistors on the FLIC but pulled down by the SFP module when the module is inserted; thus 0 is “module present” and 1 is “module absent”.

The RATESEL bits are reserved for identification of multi-speed transceivers.

SSB EMULATOR U2 : ADDRESSES 105 - 108 : GTX112 USER RUN NUMBER

These registers read back the User Run Number counter from each Core Crate Emulator in GTX112.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	User Run Number															

The Core Crate Emulator code implements a User Run Number that is part of the SSB data. As of 20150605, a fixed value of 0x12345678 is used as the ROBIN has problems with the run number incrementing. When/if an incrementing or user-programmable User Run Number is added to the firmware, these four registers will read the current value of the User Run Number.

SSB EMULATOR U2 : ADDRESSES 109 – 10C : GTX112 Level 1 ID

These registers read back the lower 16 bits of the Level 1 ID counter from each Core Crate Emulator in GTX112.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	User Level 1 ID															

The Core Crate Emulator code implements a 32-bit Level 1 ID value that can take various forms depending upon various control bits, but is in general a counter that increments each record. The user may read the lower 16 bits of the Level 1 ID value from each Core Crate Emulation block of GTX112 in these registers.

SSB EMULATOR U2 : ADDRESSES 109 – 10C : GTX112 Status

These registers read back four status bits from each of the four links in GTX112.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Link 3				Link 2				Link 1				Link 0			
RO	TX RESET DONE	RX RESET DONE	COMMA	RX BYTE ALIGN	TX RESET DONE	RX RESET DONE	COMMA	RX BYTE ALIGN	TX RESET DONE	RX RESET DONE	COMMA	RX BYTE ALIGN	TX RESET DONE	RX RESET DONE	COMMA	RX BYTE ALIGN

The Core Crate Emulator code implements a 32-bit Level 1 ID value that can take various forms depending upon various control bits, but is in general a counter that increments each record. The user may read the lower 16 bits of the Level 1 ID value from each Core Crate Emulation block of GTX112 in these registers.

SSB EMULATOR U2 : ADDRESS 200 : PULSED_CTL_REG_200

Controls GTX 112 front panel SFP links.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y3				GTX X0Y2				GTX X0Y1				GTX X0Y0			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX112_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX112_RXRESET_DONE occurring some time later.

SSB EMULATOR U2 : ADDRESS 201 : PULSED_CTL_REG_201

Controls GTX 112.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	Enable SSB Data(3:0)				Enable FIFO Data(3:0)				FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- Bits 11:8 cause the Core Crate Emulators to send the contents of a user filled FIFO as SSB record data. It is assumed the records were properly formatted by the software that filled the FIFO.
- Bits 15:12 cause the Core Crate Emulators to generate a series of SSB Records using various counters, PRBS data, and the contents of the Number of Records and Record Delay registers.

SSB EMULATOR U2 : ADDRESS 202 : PULSED_CTL_REG_202

Reserved for controlling GTX 113 links. Mapping would be identical to Address 200.

SSB EMULATOR U2 : ADDRESS 203 : PULSED_CTL_REG_203

Reserved for controlling GTX 113 features. Mapping would be similar to Address 201.

SSB EMULATOR U2 : ADDRESS 204 : PULSED_CTL_REG_204

Reserved for controlling GTX 114 links. Mapping would be identical to Address 200.

SSB EMULATOR U2 : ADDRESS 205 : PULSED_CTL_REG_205

Reserved for controlling GTX 114 features. Mapping would be similar to Address 201.

SSB EMULATOR U2 : ADDRESS 206 : PULSED_CTL_REG_206

Reserved for controlling GTX 115 links. Mapping would be identical to Address 200.

SSB EMULATOR U2 : ADDRESS 207 : PULSED_CTL_REG_207

Reserved for controlling GTX 115 features. Mapping would be similar to Address 201.

SSB EMULATOR U2 : ADDRESS 208 : PULSED_CTL_REG_208

Controls GTX116 (RTM)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y19				GTX X0Y18				GTX X0Y17				GTX X0Y16			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX116_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX116_RXRESET_DONE occurring some time later.

SSB EMULATOR U2 : ADDRESS 209 : PULSED_CTL_REG_209

Controls GTX116 (RTM)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	X	X	X	X	X	X	X	X	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.

SSB EMULATOR U2 : ADDRESS 20A,20B,20C,20D,20E,20F : UNUSED

DEFAULT VALUE AT POWER-UP : 0x0000.

FLIC FPGA U3 (Data Collector)

In the final implementation of the FLIC FPGAs U3 and U4 act as data collector objects, receiving the data streams from U1 and U2, merging event fragments and sending those merged fragments to processor blades in the ATCA shelf for monitoring or alternate triggering purposes. A second function of FPGA U3 is the control of the reference clock chip that is used by FPGAs U1 and U2 for the front panel SFP links.

FPGA U3: ADDRESS 000 : SFP_CLOCK_CONTROL_REG

For U3, the SFP_Clock Control register controls the pins of the clock generator that provides the reference clock for all front panel SFP SERDES links in both U1 and U2.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	PR1	PR0	X	OD2	OD1	OD0	X	X	OS1	OS0	X	X	RST	CE

This register sets the operational parameters of the clock generator chip. We have a 25MHz crystal. Selections that make sense for a 25MHz input are as follows. The nominal FLIC settings are highlighted (orange for 2Gbps, green for 3Gbps).

Fin(MHz)	Feedback	Prescale	PR1/0	VCO	Odiv	Fout	ExpectedUse
25	15	5	01	1875	8(111)	46.875	
25	15	5	01	1875	6(101)	62.5	1Gbps_raw_8b/10b
25	20	4	11	2000	8(111)	62.5	1Gbps_raw_8b/10b
25	24	3	00	1800	8(111)	75	
25	25	3	10	1875	8(111)	78.125	
25	20	4	11	2000	6(101)	83.333	
25	15	5	01	1875	4(011)	93.75	
25	24	3	00	1800	6(101)	100	
25	25	3	10	1875	6(101)	104.167	
25	15	5	01	1875	3(010)	125	2Gbps_raw_8b/10b_(Slink_current)
25	20	4	11	2000	4(011)	125	2Gbps_raw_8b/10b_(Slink_current)
25	24	3	00	1800	4(011)	150	
25	25	3	10	1875	4(011)	156.25	10G_Ethernet_3.125Gb/s_raw_8b/10b
25	20	4	11	2000	3(010)	166.667	
25	15	5	01	1875	2(001)	187.5	3Gbps_raw_8b/10b
25	24	3	00	1800	3(010)	200	DDR_Reference_Clock
25	25	3	10	1875	3(010)	208.333	
25	20	4	11	2000	2(001)	250	4Gbps_raw_8b/10b
25	25	3	10	1875	2(001)	312.5	5Gbps_raw_8b/10b
25	15	5	01	1875	1(000)	375	Aurora_6Gbps_raw_8b/10b
25	20	4	11	2000	1(000)	500	
25	24	3	00	1800	1(000)	600	
25	25	3	10	1875	1(000)	625	

The two PR pins define the prescaler divider as well as the feedback divider. The FLIC normal setting is highlighted.

CONTROL INPUTS		PRESCALER	FEEDBACK	PFD FREQUENCY	
PR1	PR0	DIVIDER	DIVIDER	MINIMUM	MAXIMUM
0	0	3	24	24.305	28.47
0	1	5	15	23.33	27.33
1	0	3	25	23.33	27.33
1	1	4	20	21.875	25.62

The three OD pins define the output divider:

OD2	OD1	OD0	OUTPUT DIVIDER
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	Reserved
1	0	1	6
1	1	0	Reserved
1	1	1	8

The two OS pins define the output TYPE. The correct setting for all frequencies in the FLIC is LVDS.

CONTROL INPUTS			
OS1	OS0	OUTPUT TYPE	
0	0	LVCMOS	OSC_OUT Off
0	1	LVDS	OSC_OUT Off
1	0	LVPECL	OSC_OUT Off
1	1	LVPECL	OSC_OUT On

The CE (the data sheet for the clock chip refers to is as “output enable”) is active HIGH. If the CE pin is low, outputs are all high-Z. The RESET is active low. A 0->1 edge resets the PLL, then the '1' level lets the chip run. To load new parameters into the clock chip, the OD, OS and PR pins are first set up and then the RESET pin is toggled low, then back high again.

USAGE

Normally this register is left untouched. Immediately upon coming active after programming U3, a state machine first asserts CE=0, RESET=1. After 20ns, the state is changed to CE=1, RESET=0. After a delay of 5.12us, the state is finalized at CE=1, RESET=1 and the clock generator should be active. In the initial state machine setup of the clock generator, the PR, OD and OS bits are hard-coded to OD=”011” and PR=”11”, the setting for 2Gbps operation.

Procedure to manually change SFP clock frequency

Should the user wish to change the setting of the clock generator, the SFP_CLOCK_CONTROL register should first be set with the correct values in the PR, OD and OS fields, and also with both the CE and RESET bits high. For 3Gpbs operation the correct initial value is 0x1113. After setting the SFP_CLOCK_CONTROL register, the user then performs the following sequence:

1. Set bit 0 of the GENERAL_CTL register to enable manual control of the clock generator. The value of the SFP_CLOCK_CONTROL register is immediately asserted onto the clock generator pins. The default value of 0x1113 sets CE=1, RESET=1.
2. Write the SFP_CLOCK_CONTROL register with the correct value for PR, OD and OS, but set the RESET bit *low* and the CE bit *high*. (e.g., 0x1111 for 3Gbps).
3. Write the SFP_CLOCK_CONTROL register to toggle the RESET bit back high (e.g. 0x1113).
4. Finally, enable the clock generator to drive the new frequency by setting the RESET bit high and the CE bit *low* in the SFP_CLOCK_CONTROL register. (e.g., 0x1112).

DEFAULT VALUE AT POWER UP : 0x1113. This is the correct initial setting to allow the user to manually switch to 3Gbps operation.

FPGA U3: ADDRESS 001 : LED_REG

Generic diagnostic register allowing the user to play with two of the board's LEDs. Same functionality as U1 and U2, but different LEDs. U3 drives LEDs 9 and 8. LED8 is connected to a counter to make it blink just as a visual indicator that there is valid code in U3.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	X	X	LED9	X

USAGE

There is little to do with this register at present. It is provided for future expansion of LED functionality.

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 002 : GENERAL_CONTROL_REG

Generic control register allowing the user to override automatic settings.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	X	X	ETH CLK	SFP CLK

BIT DESCRIPTIONS

- Bit 0, if clear, leaves control of the external clock chip that sets the rate of U1's and U2's front panel SFP links to the startup state machine. Otherwise, if the bit is set, this enables use of the Clock Control Register for manual control of that clock generator's frequency.
- Bit 1, if clear, leaves control of the external clock chip that sets the rate of U3's and U4's Ethernet interfaces to the startup state machine. Otherwise, if the bit is set, this enables use of the Clock Control Register for manual control of that clock generator's frequency.

DEFAULT VALUE AT POWER-UP: 0x0000.

USAGE NOTES

U3 controls a clock generator that affects what goes on in both U1 and U2. It is critically important to set the SFP clock speed before attempting any form of communication with the SSB module.

FPGA U3: ADDRESS 003 : ETHERNET_CLOCK_CONTROL_REG

For U3, the ETHERNET_CLOCK_CONTROL register controls the pins of the clock generator that provides the reference clock for all ATCA Ethernet links in both U3 and U4.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	PR1	PR0	X	OD2	OD1	OD0	X	X	OS1	OS0	X	X	RST	CE

USAGE

Normally this register is left untouched. Immediately upon coming active after programming U3, a state machine first asserts CE=0, RESET=1. After 20ns, the state is changed to CE=1, RESET=0. After a delay of 5.12us, the state is finalized at CE=1, RESET=1 and the clock generator should be active. In the initial state machine setup of the clock generator, the PR, OD and OS bits are hard-coded to OD="011" and PR="10", the setting for 10GbE operation.

Procedure to manually change Ethernet clock frequency

Should the user wish to change the setting of the clock generator, the ETHERNET_CLOCK_CONTROL register should first be set with the correct values in the PR, OD and OS fields, and also with both the CE and RESET bits high. After setting the ETHERNET_CLOCK_CONTROL register, the user then performs the following sequence:

1. Set bit 1 of the GENERAL_CTL register to enable manual control of the clock generator. The value of the ETHERNET_CLOCK_CONTROL register is immediately asserted onto the clock generator pins. The default value of 0x1113 sets CE=1, RESET=1.
2. Write the ETHERNET_CLOCK_CONTROL register with the correct value for PR, OD and OS, but set the RESET bit *low* and the CE bit *high*.
3. Write the ETHERNET_CLOCK_CONTROL register to toggle the RESET bit back high
4. Finally, enable the clock generator to drive the new frequency by setting the RESET bit high and the CE bit *low* in the ETHERNET_CLOCK_CONTROL register.

DEFAULT VALUE AT POWER UP : 0x2313. This is the correct initial setting to allow the user to manually switch to 3Gbps operation.

FPGA U3: ADDRESS 004 : GTX112_CTL_REG

Enables/disables the GTX112 inter FPGAlinks between U3 and U4.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	TDIS3	TDSI2	TDIS1	TDIS0

BIT DEFINITIONS

Each TDIS (**T**ransmitter **DIS**able) bit, if set high, disables the associated front panel fiber transmitter. The order of these bits is that bit 0 is the leftmost SFP of the four connected to a given FPGA, as viewed looking into the front panel; bit 3 is the right-most.

DEFAULT VALUE AT POWER-UP : 0x0000. This ***enables*** all the SFP modules, so the user doesn't need to do anything to send or receive data. Normally there is no need to disable unused links.

FPGA U3: ADDRESS 005 : GTX113_CTL_REG

Enables/disables the GTX113 inter FPGAlinks between U3 and U2.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	TDIS3	TDSI2	TDIS1	TDIS0

BIT DEFINITIONS

Each TDIS (**T**ransmitter **DIS**able) bit, if set high, disables the associated front panel fiber transmitter. The order of these bits is that bit 0 is the leftmost SFP of the four connected to a given FPGA, as viewed looking into the front panel; bit 3 is the right-most.

DEFAULT VALUE AT POWER-UP : 0x0000. This ***enables*** all the SFP modules, so the user doesn't need to do anything to send or receive data. Normally there is no need to disable unused links.

FPGA U3: ADDRESS 006 : GTX114_CTL_REG

Enables/disables the GTX112 inter FPGAlinks between U3 and U1.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	TDIS3	TDSI2	TDIS1	TDIS0

BIT DEFINITIONS

Each TDIS (**T**ransmitter **DIS**able) bit, if set high, disables the associated front panel fiber transmitter. The order of these bits is that bit 0 is the leftmost SFP of the four connected to a given FPGA, as viewed looking into the front panel; bit 3 is the right-most.

DEFAULT VALUE AT POWER-UP : 0x0000. This ***enables*** all the SFP modules, so the user doesn't need to do anything to send or receive data. Normally there is no need to disable unused links.

FPGA U3: ADDRESS 007 - 00A : PRBS CONTROL REGISTERS

This set of four registers defines the (Pseudo-Random Bit Sequence) PRBS control parameters. A PRBS generator is available to drive a programmable data sequence out any SERDES link. A matching PRBS receiver will lock on to the pattern and compare received data to transmitted data for bit-error-rate-testing (BERT).

REGISTER 0x0007: NUMBER OF COMMAS AFTER RESET

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	INITIAL NUMBER OF COMMAS AFTER RESET															

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0020.

REGISTER 0x0008: NUMBER OF WORDS TO SEND BEFORE INSERTING COMMA(S)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Number of words to send before inserting comma character(s)															

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0040.

REGISTER 0x0009: NUMBER OF COMMAS TO SEND IN COMMA BREAKS

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	UNUSED												# of commas			

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0002.

REGISTER 0x000A: TOTAL NON-COMMA PATTERN LENGTH BEFORE PATTERN RESTART

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Number of words to send before restarting PRBS sequence.															

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0100.

The pseudo-random sequence is generated using a shift register with exclusive-or gates. In the current version of the U1 code, four PRBS generators and four PRBS receivers are connected to the four SERDES units associated with the four front panel SFP connections. The seed values for each PRBS are different, stored in registers at addresses 0x000C, 0x000D, 0x000E and 0x000F. The default seeds are 0x0135, 0x1234, 0x5678 and 0xF18A. A PRBS spreadsheet in the code repository may be used to generate the expected data stream for any seed.

FPGA U3: ADDRESS 00B : ILA_MUX_CTL_REG

Controls operation of the multiplexed latch in the GTX instantiations preceding the ILA for the GTX quad.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X							GTX 114 MUX SEL		GTX 113 MUX SEL		GTX 112 MUX SEL	

BIT DEFINITIONS

- The GTX MUX SEL bits select which of the four SERDES links in the GTX quad is sampled for the GTX ILA. The order and format of the ILA doesn't change, just which SERDES is being monitored.
    - For GTX 112, 00:X0Y0, 01:X0Y1, 10:X0Y2, 11:X0Y3. Same relative order for other GTX quads.

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 010 : ETH1_XAUI_CTL_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 011 : ETH1_10GEMAC_TX_CONFIG_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 012 : ETH1_10GEMAC_TX_MTU_SIZE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 013 : ETH1_10GEMAC_RX_CONFIG_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 014 : ETH1_10GEMAC_RX_MTU_SIZE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 015 : ETH1_10GEMAC_PAUSE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 016 : ETH1_10GEMAC_CTL_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 017-019 : ETH1_FLIC_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 01A-01B : ETH1_FLIC_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 01C : ETH1_FLIC_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 01D-01F : ETH1_HOST_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 020-021 : ETH1_HOST_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 022 : ETH1_HOST_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 023-02F : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 030 : ETH2_XAUI_CTL_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 031 : ETH2_10GEMAC_TX_CONFIG_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 032 : ETH2_10GEMAC_TX_MTU_SIZE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 033 : ETH2_10GEMAC_RX_CONFIG_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 034 : ETH2_10GEMAC_RX_MTU_SIZE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 035 : ETH2_10GEMAC_PAUSE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 036 : ETH2_10GEMAC_CTL_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 037-039 : ETH2_FLIC_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 03A-03B : ETH2_FLIC_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 03C : ETH2_FLIC_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 03D-03F : ETH2_HOST_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 040-041 : ETH2_HOST_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 042 : ETH2_HOST_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 043-04F : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESSES 050, 051, 052, 053 : TX_SEED REGISTERS

These registers define the starting (seed) value to use in the PRBS generators (frame generators). The register at address 0x00C defines the seed for link 0 of GTX112 and also for link 0 of GTX116. TX_SEED0 defaults at power-up to 0x0135; TX_SEED1 to 0x1234, TX_SEED2 to 0x5678 and TX_SEED3 to 0xF18A.

FPGA U3: ADDRESSES 054, 055, 056, 057 : NUMBER OF TRACKS REGISTERS

These registers define the number of tracks that will be generated by each copy of the Core Crate Emulator in response to the transmit pulse control bit.

FPGA U3: ADDRESSES 058, 059, 05A, 05B : NUMBER OF RECORDS REGISTERS

These registers define the number of records that will be generated by each copy of the Core Crate Emulator in response to the transmit pulse control bit.

FPGA U3: ADDRESSES 05C, 05D, 05E, 05F : RECORD DELAY REGISTERS

These registers define the delay in clocks between records that will be generated by each copy of the Core Crate Emulator in response to the transmit pulse control bit.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	RND	RECORD DELAY(14:0)														

BIT DEFINITIONS

- The RND bit selects between a random or fixed delay between records. If RND is set, the delay is random. If RND is clear, the delay is fixed.:X0Y2, 11:X0Y3.
- The RECORD DELAY parameter is the fixed delay used between records when RND is clear.

FPGA U3: ADDRESSES 060-061 : FIFO112 PROG THRESHOLDS

Registers 0x0060 and 0x0061 define the Programmable Empty and Programmable Full thresholds of the GTX112 input FIFOs

FPGA U3: ADDRESSES 062-063 : FIFO113 PROG THRESHOLDS

Registers 0x0062 and 0x0063 define the Programmable Empty and Programmable Full thresholds of the GTX113 input FIFOs

FPGA U3: ADDRESSES 064-065 : FIFO114 PROG THRESHOLDS

Registers 0x0064 and 0x0065 define the Programmable Empty and Programmable Full thresholds of the GTX114 input FIFOs

FPGA U3: ADDRESS 066-06F : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 100 : SFP CLOCK GENERATOR STATUS

Read only status register displaying the current settings of the control bits to the SFP (front panel) clock generator chip.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	X	X	X	X	X	X	PR1	PR0	X	OD2	OD1	OD0	X	X	OS1	OS0

This register reads back the settings of the PR (prescale), OD (output divider) and OS (output select) pins as they are being driven to the SFP clock generator chip. Use the tables below to decode the setting. The expected settings that can be set by the user through the Clock Control register are highlighted in yellow. Note, in the Odiv column, that the division *factor* is not the same as the Odiv *setting*. The 3 bit code read back in the register is the *setting*, shown in the table as the value in parentheses.

Fin(MHz)	Feedback	Prescale	PR1/0	VCO	Odiv	Fout	ExpectedUse
25	15	5	01	1875	8(111)	46.875	
25	15	5	01	1875	6(101)	62.5	1Gbps_raw_8b/10b
25	20	4	11	2000	8(111)	62.5	1Gbps_raw_8b/10b
25	24	3	00	1800	8(111)	75	
25	25	3	10	1875	8(111)	78.125	
25	20	4	11	2000	6(101)	83.333	
25	15	5	01	1875	4(011)	93.75	
25	24	3	00	1800	6(101)	100	
25	25	3	10	1875	6(101)	104.167	
25	15	5	01	1875	3(010)	125	2Gbps_raw_8b/10b_(Slink_current)
25	20	4	11	2000	4(011)	125	2Gbps_raw_8b/10b_(Slink_current)
25	24	3	00	1800	4(011)	150	
25	25	3	10	1875	4(011)	156.25	10G_Ethernet_3.125Gb/s_raw_8b/10b
25	20	4	11	2000	3(010)	166.667	
25	15	5	01	1875	2(001)	187.5	3Gbps_raw_8b/10b
25	24	3	00	1800	3(010)	200	DDR_Reference_Clock
25	25	3	10	1875	3(010)	208.333	
25	20	4	11	2000	2(001)	250	4Gbps_raw_8b/10b
25	25	3	10	1875	2(001)	312.5	5Gbps_raw_8b/10b
25	15	5	01	1875	1(000)	375	Aurora_6Gbps_raw_8b/10b
25	20	4	11	2000	1(000)	500	
25	24	3	00	1800	1(000)	600	
25	25	3	10	1875	1(000)	625	

The two OS pins define the output TYPE. The correct setting for all frequencies in the FLIC is LVDS.

CONTROL INPUTS			
OS1	OS0	OUTPUT TYPE	
0	0	LVCMOS	OSC_OUT Off
0	1	LVDS	OSC_OUT Off
1	0	LVPECL	OSC_OUT Off
1	1	LVPECL	OSC_OUT On

FPGA U3 : ADDRESS 101-10F : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 110 : ETH1_XAUI_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 111 : ETH1_10GEMAC_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 112 : ETH1_10GEMAC_TX_STATISTICS_0_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 113 : ETH1_10GEMAC_TX_STATISTICS_1_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 114 : ETH1_10GEMAC_RX_STATISTICS_0_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 115 : ETH1_10GEMAC_RX_STATISTICS_1_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 116-118 : ETH1_RX_DEST_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 119-11A : ETH1_RX_DEST_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 11B : ETH1_RX_DEST_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 11C-11E : ETH1_RX_SRC_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 11F-120 : ETH1_RX_SRC_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 121 : ETH1_RX_SRC_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 122 : ETH1_RX_UDP_VALUE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 123 : ETH1_TX_IP_CHECKSUM_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 124 : ETH1_TX_IP_LENGTH_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 125 : ETH1_TX_IP_NUMBER_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 126-12F : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 130 : ETH2_XAUI_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 131 : ETH2_10GEMAC_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 132 : ETH2_10GEMAC_TX_STATISTICS_0_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 133 : ETH2_10GEMAC_TX_STATISTICS_1_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 134 : ETH2_10GEMAC_RX_STATISTICS_0_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 135 : ETH2_10GEMAC_RX_STATISTICS_1_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 136-138 : ETH2_RX_DEST_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 139-13A : ETH2_RX_DEST_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 13B : ETH2_RX_DEST_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 13C-13E : ETH2_RX_SRC_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 13F-140 : ETH2_RX_SRC_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 141 : ETH2_RX_SRC_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 142 : ETH2_RX_UDP_VALUE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 143 : ETH2_TX_IP_CHECKSUM_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 144 : ETH2_TX_IP_LENGTH_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 145 : ETH2_TX_IP_NUMBER_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 146-14F : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 150-153 : GTX112_RX_ERROR_COUNT REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 154-157 : GTX112_USER_RUN_NUMBER REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 158-15B : GTX112_USER_LEVEL_1_ID REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 15C : GTX112_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 15D-15E : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 15F : GTX112_MONITOR_FIFO_DOUT

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 160-163 : GTX113_RX_ERROR_COUNT REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 164-167 : GTX113_USER_RUN_NUMBER REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 168-16B : GTX113_USER_LEVEL_1_ID REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 16C : GTX113_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 16D-16E : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 16F : GTX113_MONITOR_FIFO_DOUT

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 170-173 : GTX114_RX_ERROR_COUNT REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 174-177 : GTX114_USER_RUN_NUMBER REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 178-17B : GTX114_USER_LEVEL_1_ID REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 17C : GTX114_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 17D-17E : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 17F : GTX114_MONITOR_FIFO_DOUT

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 200 : PULSED_CTL_REG_200

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 201 : PULSED_CTL_REG_201

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 202 : ETH1_PULSED_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 203 : ETH2_PULSED_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 204 : GTX112_PULSED_REG_0

Controls GTX 112 front panel SFP links.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y3				GTX X0Y2				GTX X0Y1				GTX X0Y0			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX112_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX112_RXRESET_DONE occurring some time later.

FPGA U3 : ADDRESS 205 : GTX112_PULSED_REG_1

Controls GTX 112.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	Enable SSB Data(3:0)				Enable FIFO Data(3:0)				FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- Bits 11:8 cause the Core Crate Emulators to send the contents of a user filled FIFO as SSB record data. It is assumed the records were properly formatted by the software that filled the FIFO.
- Bits 15:12 cause the Core Crate Emulators to generate a series of SSB Records using various counters, PRBS data, and the contents of the Number of Records and Record Delay registers.

FPGA U3 : ADDRESS 206 : GTX113_PULSED_REG_0

Controls GTX 113 front panel SFP links.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y3				GTX X0Y2				GTX X0Y1				GTX X0Y0			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL	TX RST	TX PLL	RX RST	RX PLL	TX RST	TX PLL

										RST		RST		RST		RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX113_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX113_RXRESET_DONE occurring some time later.

FPGA U3 : ADDRESS 207 : GTX113_PULSED_REG_1

Controls GTX 113.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	Enable SSB Data(3:0)				Enable FIFO Data(3:0)				FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- Bits 11:8 cause the Core Crate Emulators to send the contents of a user filled FIFO as SSB record data. It is assumed the records were properly formatted by the software that filled the FIFO.
- Bits 15:12 cause the Core Crate Emulators to generate a series of SSB Records using various counters, PRBS data, and the contents of the Number of Records and Record Delay registers.

FPGA U3 : ADDRESS 208 : GTX114_PULSED_REG_0

Controls GTX 114 front panel SFP links.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y3				GTX X0Y2				GTX X0Y1				GTX X0Y0			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX114_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.

- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX114_RXRESET_DONE occurring some time later.

FPGA U3 : ADDRESS 209 : GTX114_PULSED_REG_1

Controls GTX 114.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	Enable SSB Data(3:0)				Enable FIFO Data(3:0)				FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- Bits 11:8 cause the Core Crate Emulators to send the contents of a user filled FIFO as SSB record data. It is assumed the records were properly formatted by the software that filled the FIFO.
- Bits 15:12 cause the Core Crate Emulators to generate a series of SSB Records using various counters, PRBS data, and the contents of the Number of Records and Record Delay registers.