Current FLIC register maps REVISION 1.7

Last change: 20161019

Table of Contents

Hardware Architecture Summary

The FLIC contains four main FPGAs connected to fiber optic serial interfaces and to the ATCA backplane. The FPGAs also are connected to each other by an internal mesh of serial interfaces. Figure 1 shows a photo of a prototype FLIC connected to its rear transition module (RTM). Please note the four large FPGAs in the middle of the board (left-most FPGA has a black heat sink on it the others do not have). The left-most two ***processor*** FPGAs are connected to the silver fiber-optic interface modules at the front of the board (bottom of picture) and also to the fiber-optic interfaces mounted on the RTM.

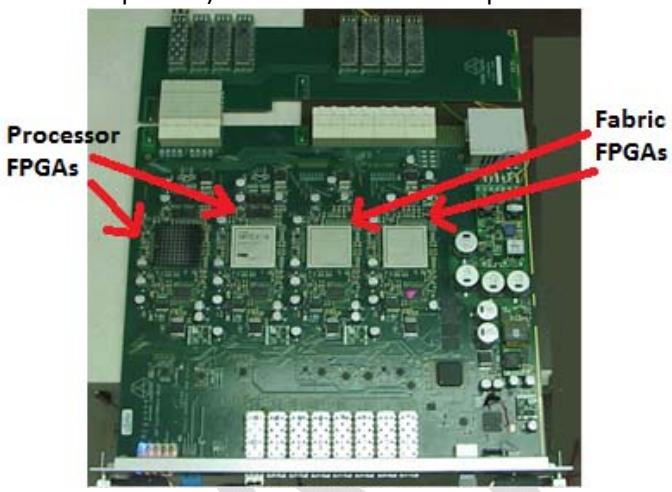

Figure 1 - Photo of prototype FLIC plus RTM.

The two large FPGAs in the center of the board, nearest the long white ATCA backplane connections, are called the ***fabric*** FPGAs. The ***processor*** FPGAs receive data though the front fiber-optic interfaces, process the data and push the results out the fiber-optic connections on the RTM. Selected subsets of data are transferred over the internal mesh of serial links from the ***processor*** FPGAs to the ***fabric*** FPGAs, who then build packets for transmission over the ATCA backplane to CPU cards, as shown in Figure 2.

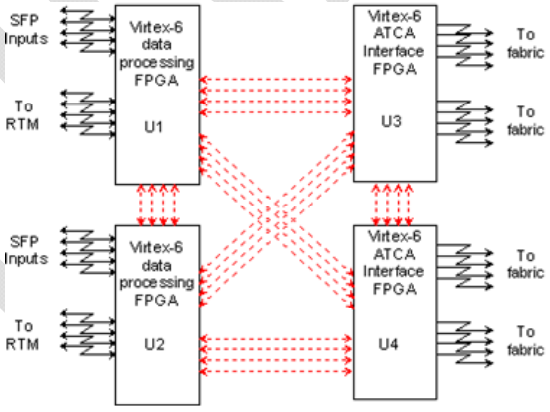

Figure 2 - Internal mesh of the FLIC.

Alternate FPGA Builds

For testing purposes, a third form of Virtex-6 firmware called the ***emulator*** has been developed that may be programmed into either or both ***processor*** FPGAs. The ***emulator*** firmware has the function of *driving* data out the fibers in the format expected by the ***processor*** firmware.

General Slow Control Structure of the FLIC

The FLIC implements five FPGAs on a shared slow control bus as shown in Figure 3. Access to the board for control or monitoring purposes is controlled by a small Management FPGA that processes read/write cycles from the PIC microcontroller. For compatibility with the ATCA standard an IPMC module connects to the PIC via a serial bus for sensor and monitoring requirements. At some future point the IPMC module may evolve to the point where the microprocessor of the IPMC may be the preferred control point, so the expansion bus of the IPMC is also connected to the Management FPGA.

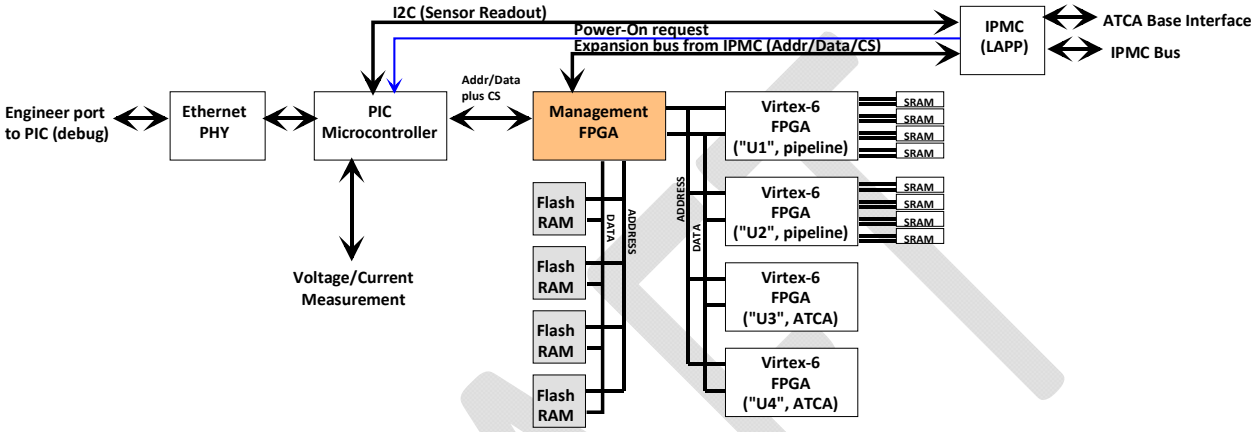

Figure 3 - Slow Control structure of FLIC

The Management FPGA firmware expects to receive single read/write transactions containing both address and data. The input side of the Management FPGA is a time-multiplexed address/data bus that is 16 bits wide. Full and complete details of the interface between PIC and Management FPGA is found in the *FLIC User's Guide*.

Data Flow Control to/from Virtex-6 FPGAs in the Management FPGA

The combination of all the internal state machines plus the requirements of PIC-FPGA, PIC-Flash, inter-FPGA, future IPMC-FPGA and/or future IPMC-Flash, a relatively complex bus control structure is required within the Management FPGA. In an effort to keep things manageable over time, a dual-rank multiplex/demultiplex scheme is employed.

In the top rank, overall control of data and control flow is determined by a two bit field FPGA_BUS_OWNER in register 0 of the Management FPGA. This two bit value determines the source of the address, data, chip select, read/write and strobe signals that define the slow control bus between the Management FPGA and the four main Virtex-6 FPGAs. The choices are summarized in Table 3.

FPGA_BUS_OWNER	Address	Data	Chip Select	Read/write	Strobe

00 (PIC)	From PIC address bus	From PIC data bus	Derived from PIC Device Select code	From PIC read/write controls	Once per PIC cycle
01 (Management FPGA internal)	From Mgmt FPGA internal mux	From Mgmt FPGA internal mux	Derived from FPGA SELECT code in list element	From Mgmt FPGA internal mux	From Mgmt FPGA internal mux
10 (IPMC)	From IPMC expansion bus	From IPMC expansion bus	From IPMC expansion bus	From IPMC expansion bus	From IPMC expansion bus
11 (inter-FPGA)	Tri-stated	Tri-stated	Tri-stated	Tri-stated	Tri-stated

Table 1 - top-level FPGA address/data/control mux

When the top-rank mux is set to allow signals from the Management FPGA internal processes (choice 01), a second-rank mux controlled by the list processor defines the internal selection. that feeds the top-level mux as summarized in Table 4.

TRANSACTION TYPE	**Address**	**Data**	**Chip Select**	**Read/write**	**Strobe**
Configuration	Held at zero	Held at zero	All off	Set to read	Held at zero
Register Load	From RegLoad state machine	From RegLoad state machine	From RegLoad state machine	From RegLoad state machine	From RegLoad state machine
SRAM Load	From SRAMLoad state machine	From SRAMLoad state machine	From SRAMLoad state machine	From SRAMLoad state machine	From SRAMLoad state machine

Table 2 - internal FPGA control signal multiplexer

Data and responses from FPGAs to Management FPGA

The data bus between FPGAs is bidirectional, and the Management FPGA implements I/O buffers. The data asserted upon the bus is continuously sampled back into the Management FPGA and the Management FPGA drivers tri-stated as needed. Similarly, the ACK signals from the four Virtex-6 FPGAs are continuously sampled.

Flash Memory Address Remapping

In the top-level multiplexer that selects between the PIC and the internal Management FPGA as the source of Flash address, a control bit allows the use of a block remapping memory within the Management FPGA. If the bit is set, the upper address bits of the Flash (block address) are not directly used but instead provide the address to a re-mapping RAM. The RAM is initialized at power-up such that each address returns itself as the data (no re-map), but the user may load a different pattern if any given Flash memory chip develops a bad block. Access to and usage of the remapping RAMs is detailed in the FLIC register map documentation.

List Processor Design Details

The Management FPGA implements three state machines that transfer information from the flash rams to the four Virtex-6 main FPGAs in different ways. These machines are referred to as the

Configuration Controller, the ***Register Loader*** and the ***SRAM Loader.*** Within the source code of the Management FPGA, these three machines are connected together in a common sub-design called ***Sub-Machines.*** This collection of machines is tied to a ***List Mux*** that is the implementation of the second-order signal mux described above in Table 4, plus a ***List Machine*** state machine that reads and executes the instructions contained in the ***List Element*** registers of the Management FPGA, as shown in Figure 3.

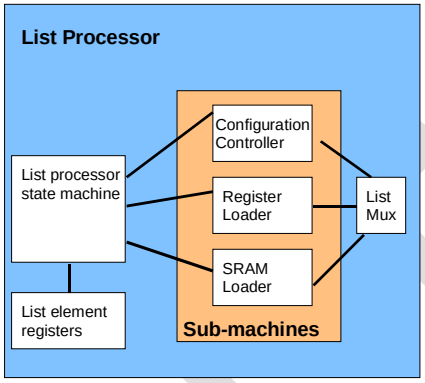

Figure 4 - the List Processor

List processor state machine Operation

The state machine within the list processor is invoked by writing a bit to a control register that tells the machine to read and process all 16 ***List Element*** registers in order. Each list element has an enable bit; if the bit is not set nothing happens and the state machine skips to the next element. Each element can invoke operation of one of the three state machines in the Sub-machines block. The list elements are always executed in order, but the user may modify the list as desired to re-execute only one or some elements again or to execute a custom list. The default power-up configuration is

- Four enabled elements that configure each of the four main FPGAs in order ("U1", then "U2", then "U3" then "U4").
- Eight additional enabled elements that, after the FPGAs are configured, load all eight SRAMs from each of the eight flash SRAM blocks.

Execution of the entire list to configure all FPGAs plus load all SRAMs typically takes about 10 seconds.

Registers within the PIC Microcontroller

Any access to the FLIC using logical target address 19 is understood to be an access to registers implemented by the firmware of the PIC microcontroller. The PIC implements 60 different registers, the great majority intended as read-only status objects.

PIC: Status Register (address 0)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	TEST STATUS VALUE															

The Status register is intended to provide a mix of status bits but at present has only two defined values:

- The value of 0xABCD is returned if the IPMC module is asserting (driving high) the power request bit.
- The value of 0x1234 is returned if the IPMC module is *not* asserting (driving low) the power request bit.

PIC: Error Register (address 1)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	FIXED VALUE of 0xEF01															

The Error register is reserved for the future implementation of PIC-specific error codes. At present it reads back the fixed value of 0xEF01 at all times.

PIC: Command Register (address 2)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Mgmt FPGA Reboot		X	X	X	X	X	X	X	X	X	X	X	x	IPMC Power Control	

BIT DEFINITIONS

Bits 1 & 0 provide a two-bit selection code that defines how the power request signal from the IPMC is processed.

- A value of “00” turns FLIC main power OFF and blocks the IPMC from changing the state of board power. This is the power-on default.
- A value of “00” turns FLIC main power ON and blocks the IPMC from changing the state of board power.
- A value of “10” or “11” hands control of the FLIC board power to the IPMC.

Bits 15 & 14 provide a soft-reboot capability for the Management FPGA. If the user writes these to “11” a signal is asserted to the Management FPGA that will cause that FPGA to reset and re-load its program.

PIC: Firmware Version Register (address 3)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	VERSION MAJOR								VERSION MINOR							

The Firmware Version register reads back the major & minor version numbers of the current firmware. For example the value 0x0307 should be interpreted as version 3.7 of the code.

PIC: TX Port Number (address 4)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	UDP PORT NUMBER USED FOR TRANSMISSION															

The TX Port number register contains the IP port number to be used by the FLIC. By fiat, the two boards used in the FTK system at CERN have been assigned port numbers 50000 and 50001 decimal.

PIC: RX Port Number (address 5)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	UDP PORT NUMBER USED FOR RECEPTION															

The RX Port number register contains the IP port number to be used by the FLIC. By fiat, FLIC boards are defined as listening on port 50000 decimal.

PIC: IP Address (addresses 6, 7)

BIT =>	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RO	Byte 4 of IP address								Byte 3 of IP address							
BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Byte 2 of IP address								Byte 1 of IP address							

The IP Address register reads back the hard-coded IP address assigned to a given FLIC. The value is set at compile time and a unique compilation of the PIC code is required for each unique FLIC installed within a subnet. Typical values used at CERN are 10.153.37.18 (USA15) and 10.193.32.17 (lab 4).

PIC: Reserved Status Registers (addresses 8-17)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Reserved, undefined															

The Reserved Status registers are reserved for future use and are at present undefined.

PIC: ADC Value Registers (addresses 18-49)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RO	X	X	X	X	X	X	ADC Conversion value

The ADC Value registers are filled with 10-bit digital values corresponding to various voltages & currents accessible by the multiplexed PIC ADC. Each of the four main FPGAs of the FLIC has an 8:1 analog multiplexer controlled by a 3-bit selection bus driven by the PIC; this results in 32 unique ADC values that may be read. The list of values available in each register is summarized in the table below. Addresses 44 through 49 are reserved for future expansion.

	Address				
Measurement	**U1**	**U2**	**U3**	**U4**	**Interpretation**
+3.3V current	12	13	14	15	Current in Amps = value read * (3.3/512)
+2.5V voltage	16	17	18	19	Voltage in Volts = value read * (3.3/1024)
+1.0V voltage	20	21	22	23	Voltage in Volts = value read * (3.3/1024)
GTX north +1.0V voltage	24	25	26	27	Voltage in Volts = value read * (3.3/1024)
GTX south +1.0V voltage	28	29	30	31	Voltage in Volts = value read * (3.3/1024)
GTX north +1.2V term. Voltage	32	33	34	35	Voltage in Volts = value read * (3.3/1024)
GTX south +1.2V term. Voltage	36	37	38	39	Voltage in Volts = value read * (3.3/1024)
Fault/ID	40	41	42	43	ID value (unique per FPGA); if less than 50 indicates fault in one or more GTX regulators. Expected values are • U1: 319 ±10 • U2: 165 ±10 • U3: 231 ±10 • U4: 287 ±10

The ADC value registers are updated either by manual request (specific command value; please refer to FLIC User's guide) or at regular intervals by setting the appropriate bit(s) in the Control register. When the IPMC module requests sensor data from the FLIC, the address of the sensor in the I2C message from the IPMC is used as an index to select which of the ADC Value registers will be returned as the sensor value.

PIC: IP Test Registers (addresses 50-55)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	IP test value															

The IP Test registers are used in engineering diagnostics and should not be read from or written to by the end user.

PIC: Diagnostic Status Registers (addresses 56-60)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Undefined diagnostic values															

The Diagnostic Status registers are used in engineering diagnostics and should not be read from or written to by the end user.

Registers within the Management FPGA

Flash Memory Sub-Architecture

Each flash memory chip consists of 128 'blocks' of data, each spanning 16k 16-bit words. The FLIC partitions each of the four flash memory chips into 8 partitions as shown in Figure 1. The main yellow area (41 blocks) contains sufficient memory (2,752,512 16-bit words) to hold the firmware image of one Virtex-6 FPGA. While we expect that in most applications of the FLIC FPGAs 'A' and 'B' will be identically programmed, and similarly that FPGAs 'C' and 'D' will be identically programmed, the flash is designed to allow each FPGA to have a unique image. This has already proven to be most valuable, as the FLIC on the test bench typically has the "data processing pipeline" code in FPGA 'A', but an "SSB Emulator" code in FPGA 'B' – because to date, no SSB board has been available for use at Argonne to send data to the FLIC.

FPGAs 'A' and 'B' both have four SRAM chips connected to them for module ID lookup when processing SSB data. Each SRAM's image is stored in the eight orange blocks of the flash map of Figure 1. After the Virtex-6 FPGAs are powered according to ATCA protocol, the Management FPGA may be commanded to copy the SRAM data from the flash to the actual SRAMs.

Other blocks in the flash memory are reserved for startup data private to the FLIC, but a number of spare blocks (colored white) are available. These may be used for board identification or tracking purposes if necessary.

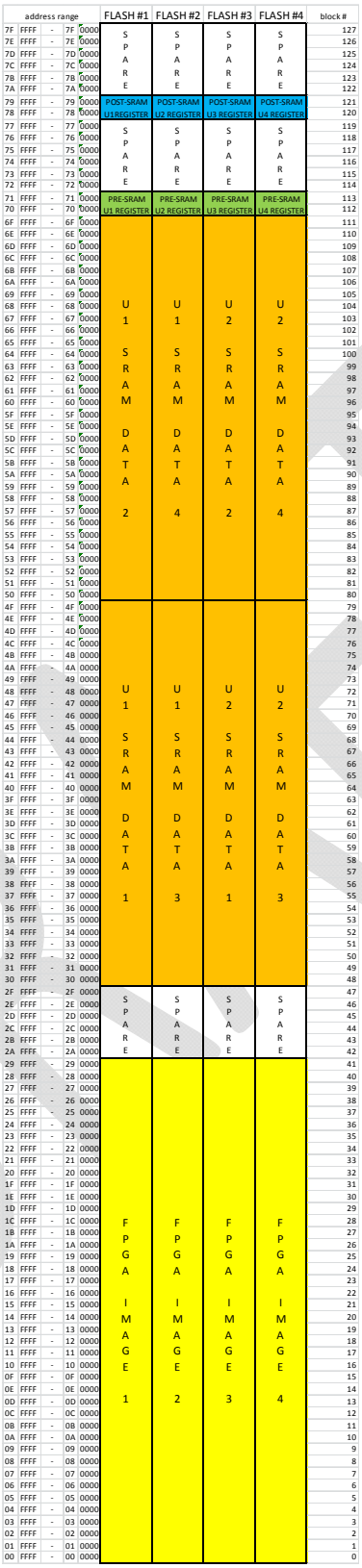

Figure 5 - Flash memory partitioning

MGMT FPGA: Control Register (address 0)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	ILA MUX SEL		FPGA Bus Owner		FPGA Bus Enbl	Flash Bus Owner	Flash Reset

BIT DEFINITIONS

- The **ILA MUX SEL** bits select which set of internal signals are connected to the Chipscope© internal logic analyzer block implemented in the Management FPGA for engineering diagnostics.
- The **FPGA Bus Owner** bits select the usage mode of the internal address/data buses that run between the Management FPGA and the four Main FPGAs. The usage coding is
    - "00" : PIC processor address/data flows to/from Main FPGAs
    - "01": Internal Management FPGA state machine address/data flows to/from Main FPGAs.
    - "10": Reserved for future implementation of address/data from the IPMC module's expansion bus (currently undefined)
    - "11": Main FPGA address/data buses are tri-stated to support future implementation of direct Main FPGA to Main FPGA data transfers. Currently the Main FPGAs do not implement this capability.
- The **FPGA Bus Enable** bit, if set, allows address, data and clock to be driven to the Main FPGAs by the Management FPGA. When the FLIC main board power is turned off this bit should also be turned off to avoid excessive current draw from the Management FPGA pins through the unpowered Main FPGAs.
- The **Flash Bus Owner** bit selects whether the flash memory address and data buses are controlled by the PIC processor (bit clear) or the internal state machines of the Management FPGA (bit set).
- The **Flash Reset** bit, if set, asserts the reset signal to all flash memory chips.

GENERAL USAGE

During the power-up sequence the PIC processor should set the **FPGA Bus Enable** bit after the power to the main FPGAs has been turned on, but before any firmware download to the Main FPGAs is initiated. If the **FPGA Bus Enable** bit is not turned on, any attempt to load firmware to the Main FPGAs will fail. The **Flash Bus Owner** bit should be set, and the **FPGA Bus Owner** bits should be set to "01", prior to enabling any of the Management FPGA's internal state machines to load firmware, copy SRAM data tables or perform register setup actions.

After board initialization is complete (all power on, all FPGAs loaded, all SRAMs loaded and all registers loaded) the **Flash Bus Owner** bit and the **FPGA Bus Owner** bits should then be reset by the PIC back to PIC control to allow general register-level access in all Main FPGAs.

DEFAULT VALUE AT POWER UP

The register initializes to 0x0000 (all control to PIC).

ANCILLIARY INFORMATION

Under normal conditions the **Flash Reset** bit is never used. This bit is only used if a programming error has left the flash ram in an unusable state.

MGMT FPGA: Flash Memory Address Remap Control Register (address 1)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	EN REMAP 3	EN REMAP 2	EN REMAP 1	EN REMAP 0

BIT DEFINITIONS

- Each of bits 3:0, if set, enables the address remapping feature of the Management FPGA for the specified flash RAM.

GENERAL USAGE

The Management FPGA implements four Address Remap RAMs, one per flash RAM. Under rare conditions a single block of flash memory can be permanently corrupted. If this occurs, the Address Remap RAM for that chip may be used to re-map addresses of the bad block to one of the unused blocks in the flash RAM so that operation of the board is not compromised. Use of the Address Remap function is transparent to the user once set up.

Each Address Remap RAM contains 128 locations (one per flash block), each loaded with a 7-bit value. By default all Remap RAMs are loaded with a data pattern where each address has its own value loaded as the data (no remap). To remap a block of flash, the location of the bad block in the remap RAM is written with the address of the different block in the flash to be used instead. The user may choose to allow the new block to be accessible at both its original and new block address, or may map the original address to somewhere else.

DEFAULT VALUE AT POWER UP

The register initializes to 0x0000 (no remapping anywhere).

MGMT FPGA: PIC Flash Address Extension Register (address 2)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	FLASH ADDRESS BITS 23:16							

GENERAL USAGE

Access of the flash memory requires a 24-bit address. Cycles from the PIC processor supply only a 16-bit address/data value. To allow the PIC to address the entire range of flash memory the upper bits of the flash address are driven by the contents of this register. The PIC firmware is coded such that access to a *logical device number* corresponding to a flash memory will utilize a transfer mechanism in which the full 24-bit address in the UDP packet is used by first writing the upper 8 bits of the packet address to this register, and then using the lower 16 bits of the address in the packet as the PIC address for a subsequent transaction to the flash memory.

DEFAULT VALUE AT POWER UP

The register initializes to 0x0000 at power-up.

MGMT FPGA: Inter-FPGA Address Extension Register (address 3)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	FPGA ADDRESS BITS			

													19:16

GENERAL USAGE

The Main FPGA address bus of the FLIC is a 20-bit object. Cycles from the PIC processor supply only a 16-bit address/data value. To allow the PIC to address the entire range of FPGA addresses the upper 4 bits of the Main FPGA address are driven by the contents of this register. The PIC firmware is coded such that access to a *logical device number* corresponding to an FPGA register will utilize a transfer mechanism in which the full 20-bit address in the UDP packet is used by first writing the upper 4 bits of the packet address to this register, and then using the lower 16 bits of the address in the packet as the PIC address for a subsequent transaction to the selected FPGA.

DEFAULT VALUE AT POWER UP

The register initializes to 0x0000 at power-up.

MGMT FPGA: Temperature Diode Control (address 4)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	D4	D3	D2	D1

GENERAL USAGE

The FLIC connects the negative side of the temperature sensing diode of each Main FPGA to the Management FPGA, while connecting the positive sides of all four diodes in parallel to a programmable resistor divider in the PIC. By programming this register the user may selectively connect any or all of the temperature diodes to ground. Setting a bit causes the diode to be grounded.

This functionality is intended as a backup temperature monitoring capability. As of this writing no PIC firmware has been developed to exploit this feature.

DEFAULT VALUE AT POWER UP

The register initializes to 0x0000 at power-up.

MGMT FPGA: ILA Address Comparison (addresses 5 & 6)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Address 5: bits 15:0 of compare value															
BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	MODE								Address 6: bits 23:16 of compare value							

GENERAL USAGE

This register is used to generate an internal signal for use with the internal diagnostic logic analyzer (Chipscope). If the MODE bit is 0, bits 19:0 of the compare value is compared against the FPGA address bus and the signal is asserted on a match. If the MODE bit is 1, bits 23:0 are used and compared against the flash RAM address value.

MGMT FPGA: List Processing Registers (addresses 0x0C – 0x1F)

Bit >	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Desc >	EN	Unused	REGION SELECT	FLASH SELECT	TRANSACTION TYPE	SRAM SELECT CODE	FPGA SELECT CODE

BIT DEFINITIONS

The fields of this register are defined as follows:

- The EN bit, if set, indicates that this list element should be processed. When the list processor is invoked it always scans all list element registers, but only performs a task if the EN bit of a given register is set.
- The Unused bits have no function and are reserved for future use.
- The REGION SELECT bit is used in concert with the FLASH SELECT and TRANSACTION TYPE bits to uniquely select an address range in the Flash RAM to read from.
    - The FLASH SELECT bit-pair simply selects which of the four Flash RAM chips is to be used.
    - The TRANSACTION TYPE, plus the REGION SELECT, define the starting/ending addresses within the Flash RAM to be used:

TRANSACTION TYPE	REGION SELECT	Address Range
00 (configure)	X – doesn't matter	0x000000 - 0x29FFFF (FPGA image area)
01 (register load)	0	0x700000 - 0x71FFFF (register area #1)
01 (register load)	1	0x780000 - 0x79FFFF (register area #2)
10 (SRAM load)	0	0x300000 - 0x4FFFFF (SRAM area #1)
10 (SRAM load)	1	0x500000 - 0x6FFFFF (SRAM area #2)
11	0	Reserved
11	1	Reserved

The SRAM SELECT code is a four-bit field used to select the upper address bits asserted to the main FPGA that is being downloaded. When writing to a main FPGA on the FLIC, the four upper address bits define how the data will be routed by the main FPGA:

- 0000 : write is to an internal register, address given by lower 16 bits of address bus.
- 0001, 0010, 0011 or 0100 : write is to one of the four SRAMs that are "behind" the FPGA. The upper 5 bits of the SRAM address come from the SRAM address extension register of the FPGA, the lower 16 from the lower 16 bits of the address bus.
- 1010 (hex 'A') : write is to all four SRAMs ('A' for "all"), all at the same address.
- 1101 (hex 'D') : write is to the DDR memory that is "behind" the FPGA. The upper 8 bits of the DDR address come from the DDR address extension register of the FPGA, the lower 16 from the lower 16 bits of the address bus.
- Other values (5,6,7,8,9,11,12,14,15) are reserved.

- The FPGA SELECT code is interpreted not as a binary value, but as a four-bit chip select vector in which each bit corresponds to one of the four Virtex-6 FPGAs of the FLIC. This allows for the possibility of downloading the same image to multiple FPGAs at the same time or loading the same SRAM table to both processor FPGAs at the same time.

GENERAL USAGE

A few typical list element values are presented here as examples.

1. A list element register set to the value 0x8001 decodes as follows:
    a. Bit 15 is set, thus the element is enabled and will be executed.
    b. Bits 12:10 are "000", selecting flash ram "00", and if needed, sub-region "A".
    c. Bits 9:8 are "00", stating that the transaction to be performed is a configuration of one or more FPGAs from a firmware image. Because of this, the sub-region value does not matter.
    d. Bits 7:4 select no SRAM, but also don't matter, because this is a configuration transaction.
    e. Bits 3:0 indicate that FPGA 1 ("U1") is to be configured.
    f. Thus, the value 0x8001 is the value used to load FPGA "U1" with firmware from the image region in the first flash ram.
2. A list element register set to the value 0x9653 (binary 1001/0110/0101/0011) decodes as follows:
    a. Bit 15 is set, thus the element is enabled and will be executed.
    b. Bits 12:10 are "101", selecting flash ram "01", and if needed, sub-region "B".
    c. Bits 9:8 are "10", stating that the transaction to be performed is configuration of SRAM chips.
    d. Bits 7:4 select SRAMs 2 and 0.
    e. Bits 3:0 indicate that FPGA 1 ("U1") and also FPGA 2("U2") are to be configured.
    f. Thus, the list element decodes to requesting that the SRAM data stored in sub-region "B" of flash ram "01" will be copied to SRAMs 2 and 0 in both FPGA1 and FPGA2. Unfortunately, this is an impossible transaction. While it would be possible to configure the same SRAM in each of two FPGAs at the same time, the SRAM selection code is illegal as it selects two SRAMs. The address extension protocol implemented does not support partial broadcasts to the SRAMs, only broadcasts to all four SRAMs.

DEFAULT VALUE AT POWER UP

The default values of the List Element registers set the Management FPGA to first load each of the four Main FPGAs with firmware, and then after firmware is loaded copy data from the Flash RAM to each of the eight SRAM lookup tables connected to FPGAs U1 and U2. Additional List Element registers are inactive but could be set to use the Register Loader state machine of the Management FPGA to perform standardized "reset" or "setup" sequences to the FPGAs.

Register	***Value***	***Action Performed***
0x0C	0x8001	Load firmware (configure) FPGA U1
0x0D	0x8402	Load firmware (configure) FPGA U2

0x0e	0x8804	Load firmware (configure) FPGA U3
0x0F	0x8C08	Load firmware (configure) FPGA U4
0x10	0x8211	Copy data from Flash 0, region A, to FPGA U1, SRAM 1
0x11	0x9221	Copy data from Flash 0, region B, to FPGA U1, SRAM 2
0x12	0x8641	Copy data from Flash 1, region A, to FPGA U1, SRAM 3
0x13	0x9681	Copy data from Flash 1, region B, to FPGA U1, SRAM 4
0x14	0x8A12	Copy data from Flash 0, region A, to FPGA U1, SRAM 1
0x15	0x9A22	Copy data from Flash 0, region B, to FPGA U1, SRAM 2
0x16	0x8E42	Copy data from Flash 1, region A, to FPGA U1, SRAM 3
0x17	0x9E82	Copy data from Flash 1, region B, to FPGA U1, SRAM 4
0x18 – 0x1F	0x0000	No action, list element inactive

MGMT FPGA: PCB Revision Register (address 0x100)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	BOARD TYPE								BOARD REVISION							

BIT DEFINITIONS

The BOARD TYPE field reads back a number indicative of what kind of ANL-HEP ATCA board this is; the FLIC has been assigned value 1. The BOARD REVISION field reads back a ordinal number indicative of which revision of the design a given board is. FLIC prototypes have a BOARD REVISION value of 0, and FLIC production boards have a BOARD REVISION value of 1.

MGMT FPGA: Firmware Revision Register (address 0x101)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	FPGA ID				REVISION MAJOR				REVISION MEDIAN				REVISION MINOR			

BIT DEFINITIONS

- The FPGA ID field indicates which FPGA within a given BOARD TYPE is being accessed. In the FLIC, the assigned FPGA ID fields are
  - 0: management FPGA
  - 1,2,3,4 : Main FPGAs U1 – U4 respectively
- The REVISION MAJOR, REVISION MEDIAN and REVISION MINOR fields are used to encode the revision of firmware in use; e.g. 7.4.1.

MGMT FPGA: Code Year Register (address 0x102)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	BCD YEAR THOUSANDS				BCD YEAR HUNDREDS				BCD YEAR TENS				BCD YEAR ONES			

BIT DEFINITIONS

The four fields of the register indicate, in binary coded decimal, the year of the firmware revision; for example, the value 0x2014 would indicate code written in the year 2014.

MGMT FPGA: Code Month/Day Register (address 0x103)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	BCD MONTH TENS				BCD MONTH ONES				BCD DAY TENS				BCD DAY ONES			

BIT DEFINITIONS

The four fields of the register indicate, in binary coded decimal, the month and day of the firmware revision; for example, the value 0x0712 would indicate code dated July 12th.

MGMT FPGA: Reserved (address 0x104)

MGMT FPGA: ATCA Hardware Address Register (address 0x105)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	0	0	0	0	0	0	0	0	PAR	ATCA Hardware Address						

BIT DEFINITIONS

The Hardware Address field reads back the number of the slot in the ATCA shelf the FLIC is in from the hard-wired lines of the backplane. The PAR bit returns the state of the Hardware Parity line of the ATCA backplane.

MGMT FPGA: List Processor Status Registers (address 0x106 – 0x10F)

The block of registers from address 0x0106 through address 0x010F provide status of the state and operation of the list processing state machines (Configurator, SRAM Loader, Register Loader). The registers at addresses 0x106 and 0x107 are currently reserved and always read back 0. Registers 0x108 through 0x10B provide overall status from a Main FPGA-centric viewpoint with address 0x108 associated with FPGA “U1”, 0x109 with “U2”, etc.

In contrast, the registers at addresses 0x10C through 0x10F provide *machine-centric* status.

- The register at address 0x10C provides status of the overall list processing state machine.
- The register at address 0x10D provides additional status of the FPGA Configurator state machine.
- The register at address 0x10E provides additional status of the Register Loader state machine.
- The register at address 0x10F provides additional status of the SRAM Loader state machine.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

x106	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
x107	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
x108	Reg Load Bus Req	CONF FLAG	RegLoad ERR	RegLoad CPLT	SRAM LOAD COMPLETE				CONF INIT HIGH	CONF INIT LOW	CONF DONE ERR	CONF CPLT	0	0	INIT	DONE
x109	Reg Load Bus Req	CONF FLAG	RegLoad ERR	RegLoad CPLT	SRAM LOAD COMPLETE				CONF INIT HIGH	CONF INIT LOW	CONF DONE ERR	CONF CPLT	0	0	INIT	DONE
x10A	Reg Load Bus Req	CONF FLAG	RegLoad ERR	RegLoad CPLT	SRAM LOAD COMPLETE				CONF INIT HIGH	CONF INIT LOW	CONF DONE ERR	CONF CPLT	0	0	INIT	DONE
x10B	Reg Load Bus Req	CONF FLAG	RegLoad ERR	RegLoad CPLT	SRAM LOAD COMPLETE				CONF INIT HIGH	CONF INIT LOW	CONF DONE ERR	CONF CPLT	0	0	INIT	DONE
x10C	Unused; read 0											ACT	Flash Status Bits			
x10D	Unused; read 0										SEL FPGA DONE	SEL FPGA INIT	Configurator state monitor			
x10E	Unused; read 0										RegLd CPLT	RegLd ERR	RegLd CPLT ACK	RegLoader state monitor		
x10F	Unused; read 0								FPGA ACK	ACT	SRAM CPLT	SRAM ERR	SRAM CPLT ACK	SRAM Loader state monitor		

BIT DEFINITIONS – PER-FPGA REGISTERS

- The Reg Load Bus Req bit, if set, indicates that the Register Loader state machine is requesting control of the FPGA address/data buses to transfer data to the given FPGA.
- The CONF FLAG bit, if set, indicates that the given FPGA is being loaded with firmware.
- The Reg Load ERR bit, if set, indicates that the Register Loader failed in error. This bit is not valid unless the Reg Load Complete bit is also set, indicating that the machine has finished running.
- The SRAM LOAD COMPLETE field indicates, on a per-SRAM basis, that the SRAM Loader machine has completed its download of that SRAM.
- The CONF INIT HIGH and CONF INIT LOW bits indicate, if the CONF DONE ERR is also set, that the type of error encountered was a failure of the INIT line to be high or low at the steps in the configuration that it should be. This would typically indicate attempts to configure a non-powered FPGA.
- The CONF Complete bit is set when the Configurator machine is finished.
- The INIT and DONE bits read the current live state of the INIT and DONE bits of the given FPGA.

BIT DEFINITIONS – PER-MACHINE REGISTERS

- ACT bits, if set, indicate that the machine is currently active. Similarly, the State Monitor bits should be static when a given machine is idle but flicker about if active.
- The Flash Status bits of the register at address 0x010C are the STAT lines directly from the four Flash RAM chips and should be polled during programming or erasure of the flash RAMs.
- The SEL FPGA DONE and SEL FPGA INIT bits in register 0x010D are the DONE and INIT lines of the selected FPGA as sampled during operation of the Configurator state machine. Typically these are only of interest if there is a hardware error on the board.
- The Register Loader asserts the Complete bit when finished, and if an error is detected, also the Error bit. The Register Loader, upon completion, waits for a Acknowledge signal from the user before clearing the Complete bit.
    - Similarly, the SRAM Loader register provides access to the Complete and Error bits, and it also requires an Acknowledge to clear the Complete.

MGMT FPGA: Pulsed Control Register (address 0x200)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	LIST GO

BIT DEFINITIONS

The List Processor state machine, that reads the List Element registers and based upon them initiates activity of the Configurator, Register Loader and SRAM Loader state machined, is started by writing a '1' to the LIST GO bit of this register.

GENERAL USAGE

This register is a ***pulsed control*** register. This means that writing a '1' to the register causes an internal pulse to occur that initiates some action, but before the write cycle completes the register self-clears. Thus the register always reads back zero and it is effectively a ***write only*** register. Writing multiple bits simultaneously is allowed; if defined each bit's action will also occur simultaneously.

MGMT FPGA: Flash Address Remap RAMs (addresses 0x300 - 0x6FF)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Unused									Remap Block number						

GENERAL USAGE

The FLIC implements four Flash Address Remap RAMs, one for each Flash RAM. Each RAM has 128 locations, matching the 128 blocks in each Flash RAM. At power up the Remap RAMs are initialized such that each address contains its own value (i.e. address 27 contains 27, address 53 contains 53, etc.). Should a block of Flash RAM become corrupt and unusable the user may load the Remap RAMs with a different pattern such that the corrupt block is replaced by another.

If remapping is enabled by setting bits in the Flash Remap Enable register (address 1), the upper 7 bits of the flash RAM address are applied to the Remap RAM associated with the Flash RAM being accessed, and the output value of the RAM is used as the upper 7 bits of the Flash RAM address in place of the original upper bits. This transparently remaps one block of Flash to another.

PROCESSOR FPGA REGISTERS

The processor FPGA firmware operates as a data processing pipeline with multiple clock domains, as shown in Figure 7. In this drawing, two FPGAs are shown. At top left is an ***emulator*** FPGA that ***generates*** SSB data, a firmware build used only in testing. The much larger portion of the drawing forms a block diagram of the ***processor*** FPGA architecture. This setup is used in bench testing of a single board. In normal operation, a FLIC has both FPGAs "U1" and "U2" programmed as ***processor*** devices.

This section of the document describes all registers in the ***processor*** firmware build. A later section describes the registers of the ***emulator*** firmware build.

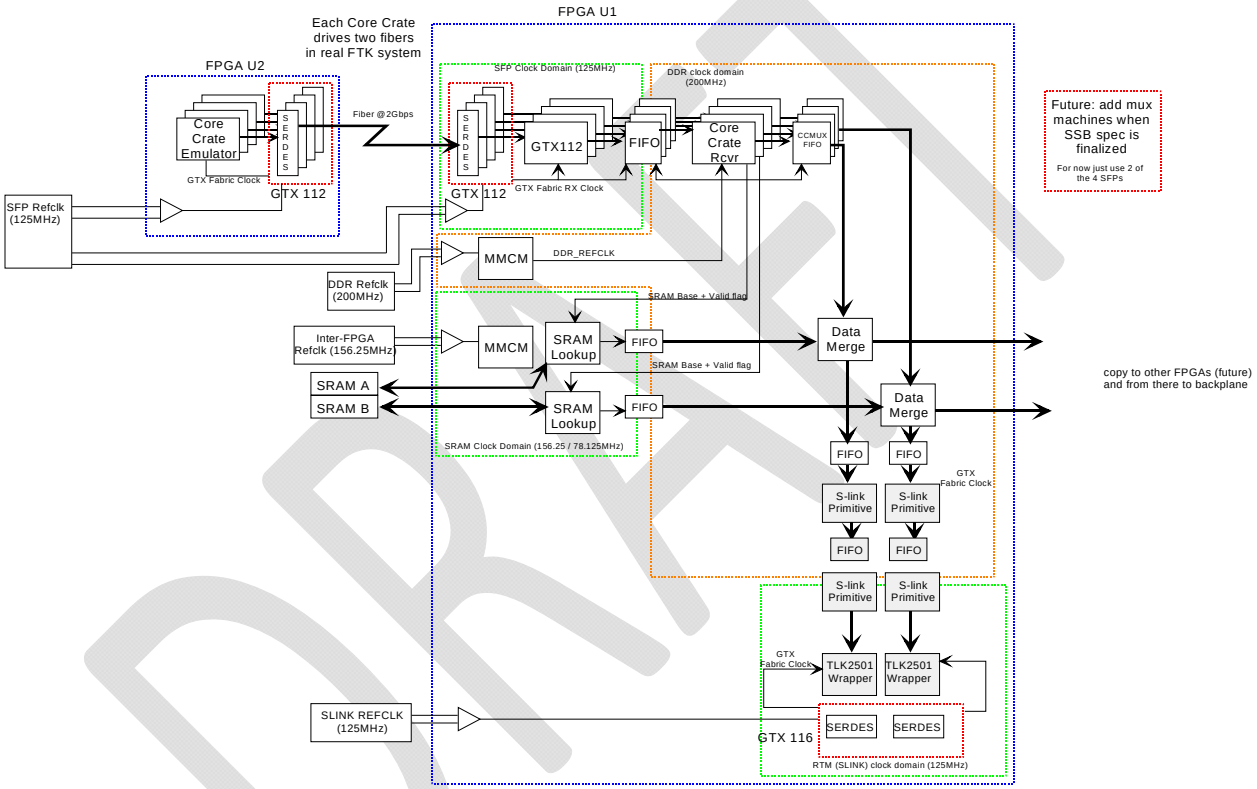

Figure 6 - FLIC Data Processing Pipeline Block Diagram

Data from the SSB (also known as a Core Crate) enters via SERDES block GTX112 and is immediately buffered into a FIFO. A Core Crate Receiver state machine, operating in a different clock domain, processes the events as they are received. A specific input data format has been agreed upon, described in the *FLIC User's Guide*. The ***processor*** firmware synchronizes to the input format, merges the input data with data from the external SRAM, and then re-formats the merged data to the S-Link format used by CERN. This document does not describe the purpose of the overall architecture and the reader is assumed to have fully read the *FLIC User's Guide* prior to reading this document. The document is limited to the details of register implementation.

PROCESSOR FPGA: ADDRESS 0x0000 : SLINK_CLOCK_CONTROL_REG

The SLINK_CLOCK_CONTROL register allows to user to control the pins of the clock generator that provides the reference clock for all S-LINK (RTM) SERDES links in both processing FPGAs. These are the SERDES links that drive the rear transition module. FPGAs "U1" and "U2" are designed to implement the identical ***processor*** firmware builds, but functions associated with the S-LINK reference clock only function in FPGA "U1", as this is the chip that physically connects to the S-LINK clock generator chip (see Figure 2).

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	X	CLOCK RATE INDEX		

BIT DEFINITIONS

This register is used in conjunction with the PULSED_CTRL register located at address 0x020E. The Clock Rate Index value provides eight pre-defined control pin settings for the expected use cases:

Setting	Clock Rate	RTM SFP rate	Notes
0	62.50MHz	1Gbps	Only available in "slow" build.
1	125.00MHz	2Gbps	Only available in "slow" build.
2	156.25MHz	N/A	Rate associated with 10GbE
3	187.50MHz	3Gbps	*Beyond S-Link Specifications*
4	200.00MHz	N/A	Frequency used for DDRs
5	*250.00MHz*	*4Gbps*	*Performance not guaranteed*
6	*312.50MHz*	*5Gbps*	*Performance not guaranteed*
7	*375.00MHz*	*6Gbps*	*Performance not guaranteed*

GENERAL USAGE

Setting the Clock Rate Index value will change the reference clock rate provided to the GTX blocks of the Virtex-6 by the clock generator chip to the desired frequency, but this does ***not*** mean that the GTX will necessarily work at the clock rate selected. The GTX blocks use an internal phase locked loop (PLL) that has a limited range of operation. The frequency multiply/divide settings, determined at compile time and not at run time, specify what frequencies are possible. Alternate settings in the User Constraint File (UCF), allow for compilation of a "slow" build to support slower data rates.

DEFAULT VALUE AT POWER UP

At power up the register has the value 0x0001, which should set the clock to 125MHz. It is recommended that software perform a clock frequency setting operation as part of normal initialization to be certain that the clock generator has been set to the desired frequency.

ANCILLIARY INFORMATION

The firmware within the FPGAs of the FLIC implements the S-Link protocol using VHDL obtained from CERN. This firmware is not certified to operate at rates above 2Gbps. Operation of the S-Link at higher speeds is not guaranteed and has not been tested. To set a new clock speed, the user sets the Clock Rate Index to the desired value then performs a write to the PULSED_CTRL register located at address 0x020E to initiate a state machine that resets the external clock generator chip and sets the new frequency.

PROCESSOR FPGA: ADDRESS 0x0001 : LED_REG

Generic diagnostic register allowing the user to play with two of the board's LEDs.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	X	X	LED5	LED4

BIT DEFINITIONS

Each bit, if set, illuminates one of the front panel LEDs of the FLIC.

GENERAL USAGE

Until specific functions are associated with the two front panel LEDs associated with U1, this register allows manual control.

DEFAULT VALUE AT POWER UP

At power-up the register initializes to the value zero, turning both LEDs off.

PROCESSOR FPGA: ADDRESS 0x0002 : GENERAL_CONTROL_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	RST SRC	G116 RTX	G116 RRX	G115 RTX	G115 RRX	G114 RTX	G114 RRX	G113 RTX	G113 RRX	G112 RTX	G112 RRX	Merge En	SRAM Access	ILA SEL	CCR EN	CLK

BIT DEFINITIONS

- Bit 0, if clear, leaves control of the external clock chips to the state machines. Otherwise, if the bit is set, this enables use of the Clock Control Register for manual control.
- Bit 1, if set, enables data processing in the Core Crate Receiver machines.
- Bit 2 selects which SRAM lookup data is sampled for the General ILA
- Bit 3, if set, allows the SRAM state machine to drive the address buses to the external SRAMs. If clear, access to the SRAM via mapped slow control bus addresses is enabled.
    - Bits 3:2 of this register are connected to bits 90:89 of the general purpose ILA.
- Bit 4, if set, enables data processing in the Merge machines.
- Bits 6:5 provide the manual TX and RX resets for the frame state machines in GTX112 (front)
- Bits 8:7 provide the manual TX and RX resets for the frame state machines in GTX113 (internal)
- Bits 10:9 provide the manual TX and RX resets for the frame state machines in GTX114 (internal)
- Bits 12:11 provide the manual TX and RX resets for the frame state machines in GTX115 (internal)
- Bits 14:13 provide the manual TX and RX resets for the frame state machines in GTX116 (RTM)
- Bit 15, if clear, means that the RTX and RRX bits of this register are manual resets to the frame generator (TX) and frame checker (RX) blocks for the GTX blocks. If bit 15 is set, the resets for these units are derived from control signals from the SERDES cores.

GENERAL USAGE

Each GTX block within the FPGA has wrapped around it "PRBS frame generator" and "PRBS frame checker" state machines. The reset bits here in the GENERAL_CONTROL register are logically ORed with other bits from the various PULSED_CTRL registers to create the reset signal to the PRBS state machines. Bit 15 of the GENERAL_CONTROL register, if set, disables register control of these resets and ties the resets of the PRBS machines to the internal GTX reset signals; generally, this mode of operation is not used and not recommended.

In most GTX implementations of U1 the actual TX data is driven by a multiplexer where PRBS data is but one of the options. Each GTX has its own controls to determine how many multiplexer selections there are, found in other registers. The PRBS data generator is designed so that, while reset, it sends K28.5 comma characters.

DEFAULT VALUE AT POWER UP

0x0000.

PROCESSOR FPGA: ADDRESS 0x0003 : SLINK_CTL_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SLINK Test Pattern Enable				SLINK Reset Controller GO				SLINK TX Mux Sel				RTM TDIS			

BIT DEFINITIONS

- Bits 3:0 directly drive the TDIS lines of the four SFP modules of the rear transition module driven by the FPGA. Each bit, if ***set***, will ***disable*** the SFP unit.
- Bits 7:4 control the operation of the TX data path mux in the GTX116 logic. If the Mux Sel bit is ***clear*** *(0)*, the GTX is set to send pseudo-random test pattern data. If the bit is ***set*** *(1)*, GTX data comes from the CERN SLINK wrapper.
- Bits 10:8 are the 'GO' bits that, when set, enable the SLINK Reset Controller state machine to perform the SLINK initialization process. The SLINK logic won't do anything until the 'GO' bit is set. There is one bit per GTX in the GTX116 quad.
- Bits 15:12 are the Test Pattern Enable bits that allow the SLINK logic as given to us by CERN to send the SLINK Test Pattern.
    - *The Test Pattern Enable and 'GO' bits for a given link are mutually exclusive; don't set both at the same time.*

GENERAL USAGE

Normally this register is changed from 0x0000 to 0x00F0 by user software to select S-Link data prior to initializing communication with any S-Link receiver board. After the physical S-Link connection is present, then it is normally necessary to change the value first to 0x0FF0 to enable the reset controller to reset the CERN S-Link core, and then change the value back to 0x00F0 to start transmitting data. This is because a reset of the CERN core is necessary after the S-Link receiver stops asserting the "link down" status to remove the local "link down" status inside the FLIC.

In normal operation the upper four bits are never set, save for when some CERN engineer requests them to be set for S-Link specific diagnosis. For FLIC PRBS testing, the CERN test pattern is ***never*** used; the FLIC makes its own PRBS data stream of a different format for link testing.

DEFAULT VALUE AT POWER UP

0x0000. This means that all SFP transmitters are enabled, the TX Mux is set to PRBS data and the CERN SLINK wrapper is held reset.

PROCESSOR FPGA: ADDRESS 0x0004 : SFP_CTL_REG

This register provides controls specific to the SFP fiber interfaces of the front panel, connected to GTX block 112 within the FPGA.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	GTX112 TX MUX CTL				**T**ransmitter **DIS**able (TDIS)			

BIT DEFINITIONS

- Bits 15:8 are unused.
- Bits 7:4 are used to select the type of data transmitted by the FLIC to the SSB. Bits 7:4 control the data in front panel SFP links 3:0 of U1, respectively.
  - If a given TX MUX bit is ***set***, the FLIC sends XON / XOFF control data to the SSB.
  - If a given TX MUX bit is ***clear***, the FLIC sends PRBS test data.
- Bits 3:0 are the **T**ransmitter **DIS**able, or TDIS bits. Each TDIS bit, if set high, disables the associated front panel fiber transmitter. The order of these bits is that bit 0 is the leftmost SFP of the four connected to a given FPGA, as viewed looking into the front panel; bit 3 is the right-most.

GENERAL USAGE

Normally this register is left untouched. The TDIS bits are only used to disable transmitters for diagnostic purposes or to minimally reduce power consumption by disabling unused SFP modules. The user may opt to clear bits 7:4 during board testing to send PRBS data.

DEFAULT VALUE AT POWER UP

0x00F0. This ***enables*** all the SFP modules, so the user doesn't need to do anything to send or receive data. Similarly, all SFP links are set to be sending SSB flow control data, the default for FTK usage.

PROCESSOR FPGA: ADDRESS 0x0005 – 0x0008 : PRBS CONTROL REGISTERS

This set of four registers defines the (Pseudo-Random Bit Sequence) PRBS control parameters. A PRBS generator is available to drive a programmable data sequence out any SERDES link. A matching PRBS receiver will lock on to the pattern and compare received data to transmitted data for bit-error-rate-testing (BERT).

REGISTER 0x0005: NUMBER OF COMMAS AFTER RESET

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	INITIAL NUMBER OF COMMAS AFTER RESET															

GENERAL USAGE

Change as desired. Refer to the **Understanding the PRBS data sequence** section on page 26.

DEFAULT VALUE AT POWER UP

0x0020.

REGISTER 0x0006: NUMBER OF WORDS TO SEND BEFORE INSERTING COMMA(S)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Number of words to send before inserting comma character(s)															

GENERAL USAGE

Change as desired. Refer to the **Understanding the PRBS data sequence** section on page 26.

DEFAULT VALUE AT POWER UP

0x0040.

REGISTER 0x0007: NUMBER OF COMMAS TO SEND IN COMMA BREAKS

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	UNUSED												# of commas			

GENERAL USAGE

Change as desired. Refer to the **Understanding the PRBS data sequence** section on page 26.

DEFAULT VALUE AT POWER UP

0x0002.

REGISTER 0x0008: TOTAL NON-COMMA PATTERN LENGTH BEFORE PATTERN RESTART

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Number of words to send before restarting PRBS sequence.															

GENERAL USAGE

Change as desired. Refer to the **Understanding the PRBS data sequence** section on page 26.

DEFAULT VALUE AT POWER UP

0x0100.

The pseudo-random sequence is generated using a shift register with exclusive-or gates. In the current version of the *processor* code, four PRBS generators and four PRBS receivers are connected to the four SERDES units associated with the four front panel SFP connections. The seed values for each PRBS are different, stored in registers at addresses 0x000C, 0x000D, 0x000E and 0x000F. The default seeds are 0x0135, 0x1234, 0x5678 and 0xF18A. A PRBS spreadsheet in the code repository may be used to generate the expected data stream for any seed.

Understanding the PRBS data sequence

The PRBS design encoded within the FLIC is a self-seeding design. Upon reset, the PRBS generator sends a fixed set of comma characters for initialization then falls into an endless sequence of data. That sequence is defined by the registers at addresses 6, 7 & 8. The sequence is defined as follows:

- A set of three words of value 0x0000 defines a PRBS pattern block.
    - The first word after the three zeroes is used to seed a PRBS generator in the receiver.
- A number of PRBS words, including the seed, as defined by the value in register 6, are sent.
- After the set of PRBS words are sent, a block of commas is sent, the number defined by the value in register 7.
- The PRBS-comma-PRBS-comma… sequence continues until the total number of PRBS words as defined in register 8 have been sent.
- After the total length requirement is satisfied, a new set of three zeroes is sent and then data continues. The PRBS data continues to be generated in the transmitter so that each block is unique.

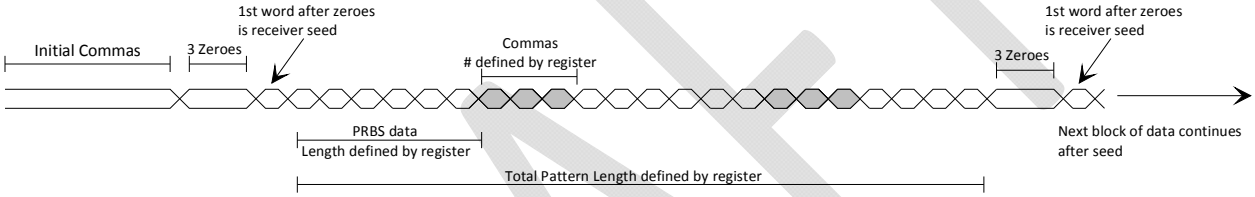

Figure 7 - PRBS data sequence.

The PRBS machines FRAME_GEN and FRAME_CHECK are not the machines generated in the example design by the Xilinx Coregen tools. They have been written specifically for the FLIC. The FRAME_GEN machine starts by sending an initial number of comma characters defined by PRBS_CONTROL(0). The machine then sends a block of exactly three words of value 0x0000, followed by a number of PRBS words. The receiving FRAME_GEN machine looks for the three words of 0x0000 (a unique value as a properly seeded PRBS will not generate 0x0000) as a starting condition for its own, separate PRBS. The first non-zero data value received after the block of three zeroes is the *seed* value that is loaded into the FRAME_CHECK machines PRBS. For all non-comma words after the seed value, the receiver's PRBS is compared against the data sent by the transmitter and all mismatches are flagged and counted. Each word after the seed is then compared against the data being received and an error flag is generated on any mismatch. An error is also flagged if the number of words with the value 0x0000 is not exactly three. Should there be an error in the transmission of the seed value, all values in the block will fail to match. To avoid an endless stream of errors stemming from one error in the seed value, the PRBS test sequence re-seeds regularly.

During the transmission of PRBS data comma characters are inserted every so often, as controlled by PRBS_CONTROL(1). The number of comma characters sent in these comma breaks is set in PRBS_CONTROL(2). An overall total data word count is kept, and then the count matches the value in PRBS_CONTROL(3) a new block of three zeroes is sent to re-seed the receiver's PRBS. The purpose of the FRAME_GEN and FRAME_CHECK machines is to provide a direct method of measuring the bit error rate of the fiber links of the FLIC.

PROCESSOR FPGA: ADDRESS 0x0009 : SLINK_CTL2_REG

This register provides ancillary controls associated with the SFP links of the rear transition module (GTX116).

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	User Global Status B				User Global Status A				FORCE LINK UP			

BIT DEFINITIONS

- Bits 15:12 are unused.
- Bits 11:8, and bits 7:4, provide two user defined status bits 'A' and 'B' (one pair per pipeline). These bits are read by the SLINK_PRIMITIVE state machine as bits 29 (user bit 'B') and 28 (user bit 'A') of the 32-bit FLIC-wide status for each event. The user bits are intended to provide a way to manually mark some events for special treatment by the ROS.
- Bit 3:0 affect the processing of data for each of the four RTM links. If set, the LDOWN* (Link DOWN) status from the S-Link logic is ignored and the data in the RTM FIFO is processed as if the S-Link was up.

GENERAL USAGE

Normally this register is left untouched, but the bits may be set to allow operation of the FLIC irrespective of the status of the S-Link receiver for diagnostic purposes or to provide test status values.

DEFAULT VALUE AT POWER-UP

0x0000. This allows normal S-Link operation.

PROCESSOR FPGA: ADDRESS 0x000A : COUNTER_CTL_REG

This register provides some general purpose bits to reset and/or control the mode of various diagnostic counters within the FLIC.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	RST	MODE	RST	MODE	RST	MODE	RST	MODE	RST	MODE	RST	MODE	X	X	X	X
	PIPELINE		GTX112		GTX113		GTX114		GTX115		GTX116		X	X	X	X

A variety of diagnostic counters are implemented within the FLIC, grouped based upon what section of the logic they monitor. On a group by group basis, the RST and MODE bits are used to control all counters within that group.

- If the RST bit is set, all counters within the group are held reset. If the RST bit is clear, the counter is free to count.
- When enabled to count, the MODE bit sets the counter mode:
  - If the MODE bit is clear, the counter simply increments whenever the signal being monitored is high.
  - If the MODE bit is set, the counter provides a *rate* measurement of how fast the counter is counting (e.g. Hz, MHz, etc.).
  - For rare events, MODE clear is usually preferred; when looking at clock rates or other common events, setting the MODE bit to see how often the event is occurring is usually chosen.

Counters in each group

The PIPELINE group contains the SRAM_REFCLK_COUNTER and DDR_REFCLK_COUNTER. These counters are typically used with the MODE bit high, to measure the speed of the SRAM and DDR clocks. The rate is sampled every microsecond so the counter value will read the frequency of the clock in MHz.

The GTX112 group contains the counters for the GTX112 REFCLK, TXCLK and RXCLK. These are normally used with MODE high, to measure the clock frequencies within this block. The rate is sampled every microsecond so the counter value will read the frequency of the clock in MHz. The GTX113, GTX114, GTX115 and GTX116 groups are handed identically.

PROCESSOR FPGA: ADDRESS 0x000B : ILA_MUX_CTL_REG

Controls operation of the multiplexed latches used to capture data prior to connection to the Chipscope internal logic analyzer.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	SRAM MUX SEL		PIPELINE MUX SEL		GTX 116 MUX SEL		GTX 115 MUX SEL		GTX 114 MUX SEL		GTX 113 MUX SEL		GTX 112 MUX SEL	

BIT DEFINITIONS

Each bit pair is associated with a different Chipscope ILA used within the FLIC firmware. As there are four processing pipelines within the FPGA, and also four SERDES links within a GTX quad, it is natural to use a two bit code per ILA for selection.

GENERAL USAGE

Set as desired to set up internal monitoring throughout the FPGA. Typically the GTX mux value will be set the same as the Pipeline mux value during FTK use so that the entire pipeline from SFP input to RTM output may be viewed. The Pipeline mux selection is common to the Core Crate Receiver, Data Merge and SLINK_PRIMITIVE machines within each pipeline.

DEFAULT VALUE AT POWER-UP : 0x0000.

PROCESSOR FPGA: ADDRESSES 0x000C through 0x000F : TX_SEED REGISTERS

These registers define the starting (seed) value to use in the PRBS generators (frame generators). The register at address 0x00C defines the seed for link 0 of GTX112 and also for link 0 of GTX116. TX_SEED0 defaults at power-up to 0x0135; TX_SEED1 to 0x1234, TX_SEED2 to 0x5678 and TX_SEED3 to 0xF18A.

PROCESSOR FPGA: ADDRESSES 0x0010 & 0x0011 : FORMAT VERSION

The registers at addresses 0x0010 (low half) and 0x0011 (high half) are used to store the 32-bit format version that the FLIC transmits in the data header out the S-Link.

DEFAULT VALUE AT POWER-UP : 0x03010000.

PROCESSOR FPGA: ADDRESSES 0x0012 through 0x0014 : GTXnnn_CTL_REG

This register provides controls specific to the SFP fiber interfaces of the front panel, connected to GTX blocks 113 through 115 within the FPGA.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	ENABLE_TIMING_TAGS				Enable FIFO			

BIT DEFINITIONS

- Bits 15:8 are unused.
- Bits 7:4 are used to enable insertion of timing tag bits into the receiving FIFO, for engineering diagnostic use only.
- Bits 3:0 select whether each SERDES line within the GTX block sends data from the TX-side FIFO (bit set), or sends PRBS test data (bit clear).

GENERAL USAGE

Typically this register is written after link integrity of the FPGA-to-FPGA link has been established by checking the PRBS data reception. After link integrity is verified, then bits 3:0 are set to enable transmission of normal data. The link can be set to send nothing but comma characters all the time by clearing the Enable FIFO bit in this register (to send PRBS data) and then additionally setting the appropriate bit in the GENERAL_CTL register to hold the PRBS machine in reset.

DEFAULT VALUE AT POWER-UP : 0x0000. This sets all four links of the GTX block to be sending PRBS test data.

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PROCESSOR FPGA: ADDRESSES 015, 016 : FLIC Error Mask registers

The two FLIC Error Mask registers together implement a 32-bit mask selecting which overall error/status conditions will result in the FLIC sending status information out the S-Link interface. This is defined in detail in the *FLIC User's Guide.*

BIT =>	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	RSV	MODE	Mask bits													
BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Mask bits															

BIT DEFINITIONS

The register at address 0x15 implements bits 15:0 of the error mask. The register at address 0x16 implements bits 31:16 of the error mask.

- Bit 31 of the 32-bit error mask is reserved for future use.
- Bit 30 of the 32-bit error mask is used to control if status is asserted upon failure of the status collection pipeline (set bit to enable).
- Bits 29 – 0 individually mask 30 different conditions that the FLIC monitors on a record-by-record basis. If a given condition is present and the mask bit for that condition is set, the S-Link formatter will send a status value to the readout system.

DEFAULT VALUE AT POWER-UP : 0x0000, 0x0000.

PROCESSOR FPGA: ADDRESSES 017 through 01E : MON_FIFO_CTL_REGs

Eight “Monitor FIFOs” allow manual capture of data at various stages of the design. These FIFOs all fill using the clock appropriate to the section of the design they monitor, but all read out using the slow control clock. Each Monitor FIFO has an associated control register to allow selection of what the input is or when a capture occurs.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	WE mode		src select	

BIT DEFINITIONS

- Bits 15:2 are unused.
- Bits 1:0 select which of the four pipelines within the processing FPGA is being monitored by the given MON_FIFO. This applies to MON_FIFOs 0,1,2 & 3. MON_FIFOs 4-7 are currently unused.
    - MON_FIFO 0 monitors data as it falls out of the CCMUX FIFO.
    - MON_FIFO 1 monitors data as it falls out of the SRAM FIFO.
    - MON_FIFO2 monitors data as it falls out of the MERGE FIFO.
    - MON_FIFO3 monitors data entering the RTM FIFO.
- Bits 3:2 select various writing modes for MON_FIFO 0 ***only***.
    - 00: capture always
    - 01: capture when data is tagged for inter-fpga transfer to U3.
    - 10: capture when data is tagged for inter-fpga transfer to U4.
    - 11: capture only if CoreCrateRcvr has flagged an error; stop when Event-End tag falls out.
- All other MON_FIFOs write all the time.

GENERAL USAGE

Different Monitor FIFOs have been connected to various points in the processing pipeline. Each FIFO’s position in the pipeline in fixed with a multiplexer to select between the pipelines. These registers, on a FIFO by FIFO basis, select which of the pipelines the given FIFO will monitor.

Each of the Monitor FIFOs is reset by writing the appropriate bit to the Pulsed Control register at address 0x020C.

DEFAULT VALUE AT POWER-UP : 0x0000. This sets all Monitor FIFOs to be monitoring pipeline 0.

PROCESSOR FPGA: ADDRESS 0x001F : HELD_RESETS_REG

General purpose control register, specifically aimed at resets. Bits set within this register are typically ORed with Pulsed Control bits to allow to user to hold some section of logic reset, as opposed to applying a pulsed reset that is immediately released.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	G116 FREAD	G116 FIFO	SLINK PRIM	MERGE	Hola Core	TLK	SRAM B	SRAM A	CCMUX FIFO resets				Core Crate Rcvr Resets			

BIT DEFINITIONS

- Bits 3:0 are pulsed resets for four Core Crate Rcvr blocks. The DDR-domain ILA monitors these bits as ILA bit 88 (section selected by ILA mux controls).
- Bits 7:4 are pulsed resets for the four CCMUX FIFOs.
- Bit 8 resets SRAM machine A; bit 9 resets SRAM machine B.
- Bit 10 resets the TLK reformatter logic from CERN in all four GTX116 copies.
- Bit 11 resets the Hola Core (S-link) logic taken from CERN in all four GTX116 copies.
- Bit 12 resets all Merge state machines and all Merge FIFOs.
- Bit 13 resets all SLINK_PRIMITIVE machines.
- Bit 14 resets all GTX 116 event FIFOs.
- Bit 15 resets all GTX 116 FIFO reader machines.

PROCESSOR FPGA: ADDRESS 0x0020 : SFP_FIFO_PROG_EMPTY_THRESH

The SFP_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the front panel SFP input FIFO, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SFP FIFO PROGRAMMABLE EMPTY THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Empty flag. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-empty at ½ the depth of the FIFO and writing 0xC000 sets the prog-empty point at ¾ of the FIFO's depth.

GENERAL USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0400. This is ¼ full.

PROCESSOR FPGA: ADDRESS 0x0021 : SFP_FIFO_PROG_FULL_THRESH

The SFP_FIFO_PROG_FULL_THRESH register sets the Programmable Full threshold of the front panel SFP input FIFO, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SFP FIFO PROGRAMMABLE FULL THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Full flag, causing the FLIC to assert the XOFF message to the SSB. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-full at ½ the depth of the FIFO and writing 0xC000 sets the prog-full point at ¾ of the FIFO's depth.

GENERAL USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0C00. This is ¾ full.

PROCESSOR FPGA: ADDRESS 0x0022 : CCMUX_FIFO_PROG_EMPTY_THRESH

The CCMUX_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the CoreCrateRcvr and Merge state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	CCMUX FIFO PROGRAMMABLE EMPTY THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Empty flag. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-empty at ½ the depth of the FIFO and writing 0xC000 sets the prog-empty point at ¾ of the FIFO's depth.

GENERAL USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0400. This is ¼ full.

PROCESSOR FPGA: ADDRESS 0x0023 : CCMUX_FIFO_PROG_FULL_THRESH

The CCMUX_FIFO_PROG_FULL_THRESH register sets the Programmable Empty threshold of the FIFO between the CoreCrateRcvr and Merge state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	CCMUX FIFO PROGRAMMABLE FULL THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Full flag, causing the FLIC to assert the XOFF message to the SSB. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-full at ½ the depth of the FIFO and writing 0xC000 sets the prog-full point at ¾ of the FIFO's depth.

GENERAL USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0C00. This is ¾ full.

PROCESSOR FPGA: ADDRESS 0x0024 : SRAM_FIFO_PROG_EMPTY_THRESH

The SRAM_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the SRAM Lookup and Merge state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SRAM FIFO PROGRAMMABLE EMPTY THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Empty flag. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-empty at ½ the depth of the FIFO and writing 0xC000 sets the prog-empty point at ¾ of the FIFO's depth.

GENERAL USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0400. This is ¼ full.

PROCESSOR FPGA: ADDRESS 0x0025 : SRAM_FIFO_PROG_FULL_THRESH

The SRAM_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the SRAM Lookup and Merge state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SRAM FIFO PROGRAMMABLE FULL THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Full flag, causing the FLIC to assert the XOFF message to the SSB. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-full at ½ the depth of the FIFO and writing 0xC000 sets the prog-full point at ¾ of the FIFO's depth.

GENERAL USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0C00. This is ¾ full.

PROCESSOR FPGA: ADDRESS 0x0026 : MERGE_FIFO_PROG_EMPTY_THRESH

The MERGE_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the Merge and SLINK_PRIMITIVE state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	MERGE FIFO PROGRAMMABLE EMPTY THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Empty flag. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-empty at ½ the depth of the FIFO and writing 0xC000 sets the prog-empty point at ¾ of the FIFO's depth.

GENERAL USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0400. This is ¼ full.

PROCESSOR FPGA: ADDRESS 0x0027 : MERGE_FIFO_PROG_FULL_THRESH

The MERGE_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the Merge and SLINK_PRIMITIVE state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	MERGE FIFO PROGRAMMABLE FULL THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Full flag, causing the FLIC to assert the XOFF message to the SSB. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-full at ½ the depth of the FIFO and writing 0xC000 sets the prog-full point at ¾ of the FIFO's depth.

GENERAL USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0C00. This is ¾ full.

PROCESSOR FPGA: ADDRESS 0x0028 : RTM_FIFO_PROG_EMPTY_THRESH

The RTM_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the SLINK_PRIMITIVE and S-Link controller state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	RTM FIFO PROGRAMMABLE EMPTY THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Empty flag. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-empty at ½ the depth of the FIFO and writing 0xC000 sets the prog-empty point at ¾ of the FIFO's depth.

GENERAL USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0400. This is ¼ full.

PROCESSOR FPGA: ADDRESS 0x0029 : RTM_FIFO_PROG_FULL_THRESH

The RTM_FIFO_PROG_EMPTY_THRESH register sets the Programmable Empty threshold of the FIFO between the SLINK_PRIMITIVE and S-Link controller state machines, allowing the user to adjust the operation of the flow control logic.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	MERGE FIFO PROGRAMMABLE FULL THRESHOLD															

BIT DEFINITIONS

The value written to the register is interpreted as the percentage of depth at which the FIFO will assert the Programmable Full flag, causing the FLIC to assert the XOFF message to the SSB. This value should be viewed as N/65536; thus, writing 0x8000 will set the prog-full at ½ the depth of the FIFO and writing 0xC000 sets the prog-full point at ¾ of the FIFO's depth.

GENERAL USAGE

Set as desired to adjust the threshold. The pipeline will have to be stopped and reset to ensure that the new threshold level takes effect.

DEFAULT VALUE AT POWER-UP : 0x0C00. This is ¾ full.

PROCESSOR FPGA: ADDRESS 0x002A/0x002B : U3_L1_ID_MATCH_REG

The U3_L1_ID_MATCH register provides a level of control over which records are tagged for copying to ATCA interface FPGA U3. The pair of registers taken together forms a 32-bit control value. The upper 16 bits are at address 0x002B, the lower 16 bits at address 0x002A.

BIT =>	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	PATT	CNT	ZERO	RSV	COUNT SEED				L1 ID Mask bits 23:16							
BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	L1 ID Mask bits 15:0															

BIT DEFINITIONS

- Bits 31:28 of the register are the MODE bits. Each mode bit, if set, enables one kind of match.
  - Bit 31 is the PATTERN match enable. If set, the L1 ID of each record is bit-by-bit ANDed with the Level 1 ID Mask bits. If the result of the AND operation is exactly zero, the record is tagged for copy to ATCA Interface FPGA U3.
  - Bit 30 is the Counter match enable. If set, the records as received are simply counted, and every nth record is copied to the ATCA Interface FPGA.
  - Bit 29 is the Zero match enable. If set, any record with an L1 ID value of exactly 0x000000 will be tagged for copy.
  - Bit 28 is reserved for future use.
- Bits 27:24 are the COUNT SEED.
  - If PATTERN mode is enabled, and a match occurs, an internal counter is loaded with the COUNT_SEED value. That number of events in a row will then be tagged for copy, after which no further records will be copied until the match fails.

- If COUNT mode is enabled, the COUNT_SEED is also used as the value for how often COUNT mode will match.
- PATTERN and COUNT modes may be used simultaneously but the single COUNT_SEED value will be used for both in two independent counters.

- Bits 23:0 are the mask value used in PATTERN mode.

GENERAL USAGE

Set as desired. Bear in mind that the Level 1 ID is a *counter*. Thus the Mask values would normally be programmed as a "one-hot" value such as 0x000010 or 0xFFFF7F. If programmed to 0x000010, any event in which bit 4 of the L1 ID is zero will match, thus matching 50% of all events (16 on, 16 off). In this case use of a small value for the COUNT_SEED is suggested, such that only one or two records every 16 are sent to the Spy Buffer logic. If the Mask value is set to 0xFFFF7F, then only the L1 ID value of 0x000080 will result in the AND equation being properly solved, and so only the COUNT_SEED number of records after L1 ID 0x000080 will be copied.

DEFAULT VALUE AT POWER-UP : 0x00000000. No records will be copied.

PROCESSOR FPGA: ADDRESS 0x002C/0x002D : U4_L1_ID_MATCH_REG

The U4_L1_ID_MATCH register works identically to the U3_L1_ID_MATCH register, save that is selects which records are copied to ATCA Interface FPGA U4 as opposed to ATCA Interface FPGA U3.

BIT =>	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	PATT	CNT	ZERO	RSV	COUNT SEED				L1 ID Mask bits 23:16							
BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	L1 ID Mask bits 15:0															

PROCESSOR FPGA: ADDRESSES 0x2E : DDR_CONTROL_REG

Engineer-only register used to control DDR memory test firmware.

PROCESSOR FPGA: ADDRESS 0x2F : SFP_FAKE_FIFO_CONTROL

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Unused								GTX112 Fake Prog Fulls				GTX112 Fake Prog Emptys			

GENERAL USAGE

PROCESSOR FPGA: ADDRESSES 0x30 – 0x35 : PIPELINE_COUNTER_CONTROLS

PROCESSOR FPGA: ADDRESS 0x100 : CODE_REVISION

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Major Revision				Minor Revision				Sub-Revision				Day Index			

GENERAL USAGE

The CODE_REVISION register provides a location to read the current version of the FLIC firmware. This register is changed when the firmware is modified to allow the user to determine if the

board contains the latest revision of firmware. The current value as of November 6, 2014 is 0x0105 (Version 0.1.0.5).

PROCESSOR FPGA: ADDRESS 0x101 : CODE_DATE_YYYY

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Year of last code revision															

GENERAL USAGE

The CODE_DATE_YYYY register provides a location to read the date, as stored by the firmware engineer, of the version of code within the FPGA.

PROCESSOR FPGA: ADDRESS 0x102 : CODE_DATE_MMDD

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Month of last code revision								Day of month of last code revision							

GENERAL USAGE

The CODE_DATE_MMDD register provides a location to read the date, as stored by the firmware engineer, of the version of code within the FPGA.

PROCESSOR FPGA: ADDRESS 0x103 : SFP_STATUS_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	LOS				MOD_PRESENT				RATESEL				TFAULT			

GENERAL USAGE

The SFP status register provides four bit-fields indicative of the state of the four front panel SFP modules connected to the FPGA. Within a four-bit group, the most significant bit is associated with the SFP furthest to the right of the group on the front panel when the board is in its normal operating orientation in the ATCA shelf.

The LOS (**L**oss **O**f **S**ignal) field reads back the loss of signal indicator from each of SFP0 through SFP3 (bit 12: SFP0, 13:1, 14:2, 15:3). The LOS bit is set if the receiving optics of the given SFP fails to detect an optical signal.

The MOD_PRESENT lines are pulled up by resistors on the FLIC but pulled down by the SFP module when the module is inserted; thus 0 is “module present” and 1 is “module absent”.

The RATESEL bits are reserved for identification of multi-speed transceivers.

The TFAULT bits, if high, indicate a transmitter fault. TFAULT is an open-collector signal requiring a pullup resistor on the FLIC to operate.

PROCESSOR FPGA: ADDRESS 0x104 : RTM_SFP_STATUS_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	LOS				MOD_PRESENT				RATESEL				0	0	0	0

GENERAL USAGE

The RTM SFP status register provides four bit-fields indicative of the state of the four rear transition module SFP units connected to the FPGA. Within a four-bit group, the most significant bit is associated with the SFP furthest to the ***left*** of the group on the panel of the RTM when the board is in its normal operating orientation in the ATCA shelf. That is, the same order (top to bottom) as the front panel SFPs.

The LOS (**L**oss **O**f **S**ignal) field reads back the loss of signal indicator from each of SFP0 through SFP3 (bit 12: SFP0, 13:1, 14:2, 15:3). The LOS bit is set if the receiving optics of the given SFP fails to detect an optical signal.

The MOD_PRESENT lines are pulled up by resistors on the FLIC but pulled down by the SFP module when the module is inserted; thus 0 is “module present” and 1 is “module absent”.

The RATESEL bits are reserved for identification of multi-speed transceivers.

PROCESSOR FPGA: ADDRESS 0x105 : CCMUX_STATUS_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	FIFO_FULLs				FIFO_EMPTYs				EVENT_CNT_OVERFLOW				EVENT_CNT_UNDERFLOW			

GENERAL USAGE

The CCMUX status register provides four bit-fields indicative of the state of the four CCMUX FIFOs in the data processing pipeline. Each four-bit field presents the same bit of information for each of the four pipelines.

- The FIFO_FULL bits are set if the CCMUX FIFO goes full. This should never happen unless the FLIC pipeline is halted by a flow control condition and an excessively large event is sent by the SSB.
- The FIFO_EMPTY bits are set if the CCMUX FIFO goes empty. This state is often true.
- The EVENT_COUNT_OVERFLOW bit is set if an error causes the number of *events* within the FIFO to overflow the internal event counter. This should be impossible under normal operating circumstances.
- The EVENT_COUNT_UNDERFLOW bit is set if an error causes the number of *events* to count down below zero, indicative that the Data Merge machine had an error and took data where none was available.

PROCESSOR FPGA: ADDRESS 0x106 : SRAM_REFCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	SRAM Reference Clock rate in MHz															

The SRAM REFCLK counter provides a measurement of the *rate* at which the SRAM machine clock is running. The rate is expressed in MHz, and the rate should be 80.

PROCESSOR FPGA: ADDRESS 0x107 : DDR_REFCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	DDR Reference Clock rate in MHz															

The DDR REFCLK counter provides a measurement of the *rate* at which the DDR clock (used as the main pipeline processing clock) is running. The rate is expressed in MHz, and the rate should be 200.

PROCESSOR FPGA: ADDRESS 0x108 : GTX112_REFCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX112 Reference Clock rate in MHz															

The GTX REFCLK counter provides a measurement of the *rate* at which the SERDES reference clock (generated by the external clock chip controlled by FPGA U3) is running. The rate is expressed in MHz, and the rate is a function of the speed at which GTX112 is set to run. For normal 2Gbps operation this is 125MHz. In a 3Gbps setup, the speed would be 187.5MHz, which would read either 187 or 188.

PROCESSOR FPGA: ADDRESS 0x109 : GTX112_TXCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX 112 TX Clock rate in MHz															

The GTX TXCLK counter provides a measurement of the *rate* at which the SERDES transmitter-side word clock is running. The rate is expressed in MHz, and the rate is a function of the speed at which GTX112 is set to run. For normal 2Gbps operation this is 125MHz. In a 3Gbps setup, the speed would be 187.5MHz, which would read either 187 or 188.

PROCESSOR FPGA: ADDRESS 0x10A : GTX112_RXCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX 112 RX Clock rate in MHz															

The GTX RXCLK counter provides a measurement of the *rate* at which the SERDES receiver-side word clock is running. This is the word clock that is derived from the data stream The rate is expressed in MHz, and the rate is a function of the speed at which GTX112 is set to run. For normal 2Gbps operation this is 125MHz. In a 3Gbps setup, the speed would be 187.5MHz, which would read either 187 or 188.

PROCESSOR FPGA: ADDRESS 0x10B : GTX116_REFCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX116 Reference Clock rate in MHz															

The GTX REFCLK counter provides a measurement of the *rate* at which the SERDES reference clock (generated by the external clock chip controlled by FPGA U1) is running. The rate is expressed in MHz, and the rate is a function of the speed at which GTX111 is set to run. For normal 2Gbps operation this is 125MHz. In a 3Gbps setup, the speed would be 187.5MHz, which would read either 187 or 188.

PROCESSOR FPGA: ADDRESS 0x10C : GTX116_TXCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX 116 TX Clock rate in MHz															

The GTX TXCLK counter provides a measurement of the *rate* at which the SERDES transmitter-side word clock is running. The rate is expressed in MHz, and the rate is a function of the speed at which GTX116 is set to run. For normal 2Gbps operation this is 125MHz. In a 3Gbps setup, the speed would be 187.5MHz, which would read either 187 or 188.

PROCESSOR FPGA: ADDRESS 0x10D : GTX116_RXCLK_COUNTER

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX 116 RX Clock rate in MHz															

The GTX RXCLK counter provides a measurement of the *rate* at which the SERDES receiver-side word clock is running. This is the word clock that is derived from the data stream The rate is expressed in MHz, and the rate is a function of the speed at which GTX116 is set to run. For normal 2Gbps operation this is 125MHz. In a 3Gbps setup, the speed would be 187.5MHz, which would read either 187 or 188.

PROCESSOR FPGA: ADDRESS 0x10E : Unused register

PROCESSOR FPGA: ADDRESS 0x10F : GTX116_RX_ERR_CNT_MUX

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	GTX 116 RX Error Counter (multiplexed)															

This register provides access to the PRBS Frame Check error counter of all four SERDES links in GTX 116. When performing PRBS link checks, the Frame Check error counter counts how many data errors were found. Bits 9:8 of the ILA_MUX_CTL_REG found at address 0x00B selects which of the four SERDES lanes of GTX 116 has its RX error counter routed out to this register. This register is *only* valid for PRBS link testing and has no meaning when the pipeline is in normal operation.

PROCESSOR FPGA: ADDRESS 0x110 – 0x11E : MONITOR FIFOs

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Various monitoring data															

Eight MONITOR FIFO registers are located at addresses 0x110, 0x112, 0x114, 0x116, 0x118, 0x11A, 0x11C and 0x11E. Due to the way the PIC parallel bus interface works there is always an unintended excess read cycle at the address *after* the selected address. Normally this is harmless but in the case of FIFOs these excess read transactions must be protected against. The FLIC thus reserves all odd-numbered register addresses from 0x111 through 0x11F as “FIFO protection addresses” that may not be used.

The actual data read from the different MONITOR FIFOs is dependent upon the settings in the various MON_FIFO_CTRL registers located at addresses 0x017 through 0x01E. As of 20150806, the MONITOR FIFOs are assigned as follows:

- MON_FIFO 0 (address 0x110) monitors the output of the CCMUX FIFO (between Core Crate Receiver and Merge state machines).
- MON_FIFO 1 (address 0x112) monitors the output of the SRAM FIFO (between SRAM lookup and Merge state machines).
- MON_FIFO 2 monitors the output of the Merge state machine.
- MON_FIFO 3 monitors the output of the SLINK_PRIMITIVE state machine.
- MON_FIFOs 4 through 7 are currently undefined.

PROCESSOR FPGA: ADDRESS 200 : PULSED_CTL_REG_200

Controls GTX 112 front panel SFP links.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y3				GTX X0Y2				GTX X0Y1				GTX X0Y0			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX112_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX112_RXRESET_DONE occurring some time later.

PROCESSOR FPGA: ADDRESS 201 : PULSED_CTL_REG_201

Controls GTX 112.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	X	X	X	X	Enable Timing Tags				FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- Bits 11:8 set flip-flops in the GTX112 PRBS Frame Check logic that will cause the *next* event to have its 'ILA TAG' set in the various FIFOs. The 'ILA TAG' is intended to allow capture of the same event at all stages of processing using the internal Chipscope analyzers.

PROCESSOR FPGA: ADDRESS 202 : PULSED_CTL_REG_202

Reserved for controlling GTX 113 links. Mapping would be identical to Address 200.

PROCESSOR FPGA: ADDRESS 203 : PULSED_CTL_REG_203

Reserved for controlling GTX 113 features. Mapping would be similar to Address 201.

PROCESSOR FPGA: ADDRESS 204 : PULSED_CTL_REG_204

Reserved for controlling GTX 114 links. Mapping would be identical to Address 200.

PROCESSOR FPGA: ADDRESS 205 : PULSED_CTL_REG_205

Reserved for controlling GTX 114 features. Mapping would be similar to Address 201.

PROCESSOR FPGA: ADDRESS 206 : PULSED_CTL_REG_206

Reserved for controlling GTX 115 links. Mapping would be identical to Address 200.

PROCESSOR FPGA: ADDRESS 207 : PULSED_CTL_REG_207

Reserved for controlling GTX 115 features. Mapping would be similar to Address 201.

PROCESSOR FPGA: ADDRESS 208 : PULSED_CTL_REG_208

Controls GTX116 (RTM)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y19				GTX X0Y18				GTX X0Y17				GTX X0Y16			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX116_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX116_RXRESET_DONE occurring some time later.

PROCESSOR FPGA: ADDRESS 209 : PULSED_CTL_REG_209

Controls GTX116 (RTM)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	X	X	X	X	User Reset Request				FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- Bits 11:8 are reset requests to the SLINK_RESET_CONTROLLER machines in GTX116. These resets combine with the SLINK Reset Controller GO bits in the SLINK_CTL register to determine what the reset state machine will do. Pulsing these bits should restart the reset sequence to an initial IDLE state, but then the GO bit has to be turned on to make the machine proceed from there.

PROCESSOR FPGA: ADDRESS 20A,20B : UNUSED

DEFAULT VALUE AT POWER-UP : 0x0000.

PROCESSOR FPGA: ADDRESS 20C : PULSED_CTL_REG_20C

Resets to Monitor FIFOs.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO	X	X	X	X	X	X	X	X	MF7 RST	MF6 RST	MF5 RST	MF4 RST	MF3 RST	MF2 RST	MF1 RST	MF0 RST

BIT DEFINITIONS

- Each of the MFx RST bits resets the associated Monitor FIFO, clearing the FIFO.
- After reset each FIFO automatically refills with new data based upon its design settings, thus writing the reset acts as an asynchronous data capture. The various Monitor FIFOs are currently set to monitor the following points in the data pipeline:
    - Monitor FIFO 0 collects the data falling out of the CCMUX FIFO, with the write enable of the Monitor FIFO set equal to the read enable of the CCMUX FIFO. MON_FIFO_CTL_REG(0) may be used to select which pipeline is monitored.
    - Monitor FIFO 1 collects the data falling out of the SRAM FIFO, with the write enable of the Monitor FIFO set equal to the read enable of the SRAM FIFO. MON_FIFO_CTL_REG(1) may be used to select which pipeline is monitored.

- Monitor FIFO 3 collects the data falling out of the MERGE FIFO, with the write enable of the Monitor FIFO set equal to the read enable of the MERGE FIFO. MON_FIFO_CTL_REG(2) may be used to select which pipeline is monitored.
- Monitor FIFO 0 collects the data being written to the RTM FIFO, with the write enable of the Monitor FIFO set equal to the write enable of the RTM FIFO. MON_FIFO_CTL_REG(3) may be used to select which pipeline is monitored.

PROCESSOR FPGA: ADDRESS 0x20D : UNUSED

DEFAULT VALUE AT POWER-UP : 0x0000.

PROCESSOR FPGA: ADDRESS 20E : PULSED_CTL_REG_20E

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO	CLKGEN RESET	X	X	X	X	X	X	X	X	X	X	X	CNTR RST 3	CNTR RST 2	CNTR RST 1	CNTR RST 0

BIT DEFINITIONS

- Bit 15 (CLKGEN RESET), forces a reset of the external SLINK (GTX 116) reference clock generator chip. See description of SLINK_CLK_CTL_REG (address 0).
- The four CNTR RST bits will cause all pipeline diagnostic counters for a given pipeline to be reset.

GENERAL USAGE

FPGAs "U1" and "U2" are designed to implement the identical ***processor*** firmware builds, but functions associated with the S-LINK reference clock only function in FPGA "U1", as this is the chip that physically connects to the S-LINK clock generator chip (see Figure 2).

PROCESSOR FPGA: ADDRESS 20F : SUBSECTION_PULSED_RESETS_REG

General purpose pulsed control register, specifically aimed at resets. This register is a pulsed version of address 0x01F.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO	G116 FREAD	G116 FIFO	SLINK PRIM	MERGE	Hola Core	TLK	SRAM B	SRAM A	CCMUX FIFO resets				Core Crate Rcvr Resets			

BIT DEFINITIONS

- Bits 3:0 are pulsed resets for four Core Crate Rcvr blocks. The DDR-domain ILA monitors these bits as ILA bit 88 (section selected by ILA mux controls).
- Bits 7:4 are pulsed resets for the four CCMUX FIFOs.
- Bit 8 resets SRAM machine A; bit 9 resets SRAM machine B.
- Bit 10 resets the TLK reformatter logic from CERN in all four GTX116 copies.
- Bit 11 resets the Hola Core (S-link) logic taken from CERN in all four GTX116 copies.
- Bit 12 resets all Merge state machines and all Merge FIFOs.
- Bit 13 resets all SLINK_PRIMITIVE machines.
- Bit 14 resets all GTX 116 event FIFOs.
- Bit 15 resets all GTX 116 FIFO reader machines.

Pass-through access to U1's external SRAM

Accesses to U1 with addresses in the range 0x10000 – 0x4FFFF will be treated as pass-through accesses to the external SRAM chips. U1 has four SRAMs (U156, U157, U159, U158) connected in two pairs. U156 and U157 are collectively referred to as "LUT1"; chips at U158/U159 are "LUT2". The two "LUTx" groups share address and data buses but have separated OE, WE and CE controls. The mapping is as follows:

- Addresses 0x10000 – 0x1FFFF provide access to U156.
- Addresses 0x20000 – 0x2FFFF provide access to U157.
- Addresses 0x30000 – 0x3FFFF provide access to U159.
- Addresses 0x40000 – 0x4FFFF provide access to U158.

Each SRAM has a 21-bit address range, larger than the window provided. The upper five bits of the address provided to the SRAM come from address extension registers, located at addresses 0x0300, 0x0301, 0x0302 and 0x0303 respectively. This provides a moveable 64K address window per SRAM, matching the 64K address space of the PIC processor.

SSB Emulation Build

Overall Data Emulation Operation

The SSB Emulation Build implements a data emulator, complementary to the standard Processor build. The data emulator generates various forms of test data for loopback testing. This data emulation module has two basic modes of operation, PRBS and FTK. The PRBS mode is designed to provide a testing pattern useful for measuring bit error rates of the serial link. The FTK mode generates data streams as expected from the SSB (Second Stage Board) of FTK, controlled by a complex state machine (the *Core Crate Emulator*).

The Emulation Build implements two complete sets of Emulator logic, one for GTX112 (the four SERDES links on the front panel) and one for GTX116 (the four SERDES links of the RTM). Historically the GTX112 side has been used much more often than the GTX116 side, but with appropriate software each FPGA programmed with the Emulator build should be able to generate 8 data streams.

The CoreCrateEmulator state machine has multiple sub-options:

- Upon reset, the state machine defaults to sending K28.5 comma characters all the time in its idle state.
- The user may load a FIFO buffer with user-defined data, and then request that the CoreCrateEmulator dump the entire contents of the FIFO before returning to idle.
- The user may set up register parameters that define machine-generated "SSB-like" events, and then ask the state machine to send those events. A single event, a burst or a never-ending sequence may be generated.

PRBS Mode

If the user sets any of bits 3:0 of the CORE_CRATE_CONTROL_REG (address 0x1F), the indexed SERDES link of GTX 112 enters PRBS mode, sending a pseudo-random testing sequence controlled by the PRBS_CONTROL registers (addresses 0x05 through 0x08) and the TX_SEED registers (addresses 0x0C through 0x0F). This is described in detail in the **Understanding the PRBS data sequence** section on page 26.

FIFO-based data

Four user FIFOs are located at addresses 0x80, 0x81, 0x82 and 0x83 (one per SFP link 0-3, in order). Each FIFO stores 16-bit data, and each FIFO is 8,192 words deep. The user FIFOs cross clock domains; they are written in the register logic clock domain but read in the GTX TX clock domain. The FIFOs, once loaded, are transmitted by setting the required bits in the PULSED_CTRL_REG at address 0x0201 (bit 11: SERDES 3; bit 10: SERDES 2; bit 9: SERDES 1; bit 8: SERDES 0). The emulation state machine must be in the idle state to send FIFO data. If the machine is not idle the FIFO is dumped when the machine next goes idle. Once the FIFO dump is initiated it continues until the FIFO is empty. Immediately upon going empty the state machine returns to the IDLE state. Thus, events larger than 8K words long may be sent as multiple packets as nothing but comma characters will be sent while the 2nd and subsequent packets are being loaded.

State Machine data

The state machine is capable of sending a wide variety of emulated events with differing numbers of tracks, various L1 ID formats and even programmable error conditions. Control over the state machine involves a large number of control registers, and so the state machine's various modes and parameters will be defined in a number of groups.

Control and operation of the emulator state machine

The state machine sends *records*, each of which may have variable numbers of *tracks*, just like the SSB data. The same pseudo-random number generator logic used for the PRBS link testing mode is also available to the state machine. The NUMBER_OF_RECORDS (addresses 0x14 – 0x17), RECORD_DELAY_CTRL (addresses 0x18 – 0x1B) and NUMBER_OF_TRACKS (addresses 0x20-0x23) registers form the main controls. There is one set of these registers per SERDES link. In the simplest case, the user loads the number of records desired into the NUMBER_OF_RECORDS register, the number of tracks per record into the NUMBER_OF_TRACKS register and the delay time between records into the RECORD_DELAY_CONTROL register. After parameters are loaded, a write to the PULSED_CONTROL register at address 0x0201 then initiates state machine data transmission.

Additional overall control bits are located in the CORE_CRATE_CONTROL register at address 0x1F. In addition to the PRBS vs. state machine mux select previously described, bits 15:12 and 11:8 allow the user to select two additional static controls on a per-link basis. The SEND LONG L1 ID bits tell the state machine to use a different format for the L1 ID field of the events and the SEND_FOREVER bits tell the state machine to run continuously until reset. See the description of the CORE_CRATE_CONTROL register for details.

A secondary control register, the CORE_CRATE_AUX_CONTROL register at address 0x2D, provides sub-selection of various L1 ID formats if the SEND LONG L1 ID bits have been set in the CORE_CRATE_CONTROL register. Other bit groups in this register enable/disable the response of the emulator to XON/XOFF messages received from the processor FPGA, select the source of error injection control and allow the user to reset the domain crossing latches that cross the clock domain boundary from the EMULATOR_ERROR_REQUEST registers at address 0x20A/0x20B/0x20C/0x20D to the SERDES state machine logic.

Event Error Injection Logic

The Core Crate Emulator state machine can, upon command, generate programmed errors in various places in the data (header, L1 ID, track, etc.). The CORE_CRATE_AUX_CONTROL register selects whether these errors are initiated by writes to the EMULATOR_ERROR_REQUEST register (allowing manual insertion of single errors) or by use of a previously loaded EMULATOR_ERROR_RAM (allowing errors of all kinds to be keyed to L1 ID values and thus allowing tests of the response to multiple errors in the same event and/or errors in adjacent events).

The types of injectable errors/conditions are

1. A *Header Error,* in which the Record Header is intentionally malformed;
2. A *Level 1 ID Error,* in which the Level 1 ID is intentionally malformed;
3. A *Level 1 ID Skip,* in which the Level 1 ID increments by two from the previous event rather than by the normal one;
4. A *Track Error,* in which the Track Header is intentionally malformed;
5. A *Layer Error,* in which the number of layers issued is incorrect;

6. A *Trailer Error,* in which the Record Trailer is intentionally malformed;
7. A *Fixed Level I ID Error,* in which the counter-based Level 1 ID is replaced by a fixed value from a register.
8. A *Zero Track Event*, in which the number of tracks controls are for one event ignored and an event with no tracks (only Record Header and Record Trailer) is produced.
9. A *Diagnostic Block Event,* in which the event contains an additional set of pseudo-random numbers, the length of which is defined by a separate control register. The default operation of the emulator is to generate a zero-length diagnostic block (0xE0DA, 0x0000, 0xE0DF, 0x0000).
    a. The emulator code as written will always generate a diagnostic block of the correct length. Expansion provisions exist to allow for the future development of an option to send a diagnostic block of incorrect length.

SSB EMULATOR: ADDRESS 000 : SLINK_CLOCK_CONTROL_REG

FPGA U2 does not control any clock generators. The SLINK Clock Control register of the Emulator build exists to copy the necessary functionality required to set up the SLINK (GTX 116) reference clocks if the FPGA at position U1 is programmed with Emulator code.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	X	Rate Index		

BIT DEFINITIONS

The **Rate Index** field is an index value that selects one of eight "standard" reference frequencies that the S-Link reference clock may be set to:

0. 62.5MHz (suitable for 1Gbps links)
1. 125MHz (default, suitable for 2Gbps links)
2. 156.25MHz (for 3.125Gbps Ethernet)
3. 187.5MHz (for 3Gbps links)
4. 200.0MHz
5. 250.0MHz (suitable for 4Gbps links)
6. 312.5MHz (suitable for 5Gbps links)
7. 375.0MHz (suitable for 6Gbps links)

GENERAL USAGE

The user should not assume that simply changing the **Rate Index** and resetting the clock will magically change the GTX to work at the new speed. Many GTX internal parameters, controlled by constraint files must also change, and this requires a recompilation. To change the clock generator speed, the new value is written to the SLINK_CLOCK_CONTROL register and then a write to PULSED_CONTROL register 0x020E is required to initiate the change.

DEFAULT VALUE AT POWER UP

0x0001, selecting a rate of 125MHz suitable for 2Gbps links.

SSB EMULATOR: ADDRESS 001 : LED_REG

Generic diagnostic register allowing the user to play with two of the board's front panel LEDs.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	X	X	LED7	LED6

BIT DEFINITIONS

Each bit, if set, causes the LED to illuminate. If the bit is clear the LED is off.

DEFAULT VALUE AT POWER UP

0x0000.

SSB EMULATOR: ADDRESS 002 : GENERAL_CTL_REG

Generic control register provided to allow the user a way to override automatic settings.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	RST SRC	G116 FGRST	G116 FCRST	X	X	G115 FGRST	G115 FCRST	G114 FGRST	G114 FCRST	G112 FGRST	G112 FCRST	X	G113 FGRST	G113 FCRST	X	SRAM SEL

BIT DEFINITIONS

- Bit 15, if clear, means that the RTX and RRX bits of this register are manual resets to the frame generator (TX) and frame checker (RX) blocks for the GTX blocks. If bit 15 is set, the resets for these units are derived from control signals from the SERDES cores.
- Bits 14:13 are the manual frame generator and frame checker resets, respectively, for GTX 116.
- Bits 10:9 are the manual frame generator and frame checker resets, respectively, for GTX 115.
- Bits 8:7 are the manual frame generator and frame checker resets, respectively, for GTX 114.
- Bits 6:5 are the manual frame generator and frame checker resets, respectively, for GTX 112.
- Bits 3:2 are the manual frame generator and frame checker resets, respectively, for GTX 113.
- Bit 0 is the SRAM address source selection bit, but as the Emulator build has no pipeline state machines setting the bit has no useful function. The address multiplexer is preserved in case the SRAMs are at some future time used in the Emulator build.

DEFAULT VALUE AT POWER UP

0x0000.

SSB EMULATOR: ADDRESS 003 : SLINK_CTL_REG

Reserved for future misuse; generally will control the TDIS pins of the rear transition module.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	ENBL TIM TAGS	RST ERR CNT	X	X	X	X	X	X	X	X	X	X	RTM TDIS			

BIT DEFINITIONS

- Bit 15, if set, enables the FRAME_CHECK machine within GTX116 (RTM) to insert ILA timing tags, used for diagnostics.
- Bit 14, if set, resets the GTX116 FRAME_CHECK machine's PRBS error counter to zero.

- Bits 3:0 directly drive the TDIS lines of the four SFP modules of the rear transition module driven by the FPGA. Each bit, if ***set***, will ***disable*** the SFP unit.

DEFAULT VALUE AT POWER UP

0x0000.

SSB EMULATOR: ADDRESS 004 : SFP_CTL_REG

Enables/disables the SFP fiber interfaces on the front panel.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	ENBL TIM TAGS	RST ERR CNT	X	X	X	X	X	X	X	X	X	X	TDIS3	TDSI2	TDIS1	TDIS0

BIT DEFINITIONS

- Bit 15, if set, enables the FRAME_CHECK machine within GTX112 (front panel SFPs) to insert ILA timing tags, used for diagnostics.
- Bit 14, if set, resets the GTX 112 FRAME_CHECK machine's PRBS error counter to zero.
- Bits 3:0 directly drive the TDIS lines of the four SFP modules on the front panel of the FLIC driven by the FPGA. Each bit, if ***set***, will ***disable*** the SFP unit.

DEFAULT VALUE AT POWER UP

0x0000**.**

SSB EMULATOR: ADDRESS 005 - 008 : PRBS CONTROL REGISTERS

This set of four registers defines the (Pseudo-Random Bit Sequence) PRBS control parameters of the FRAME_GEN machines in ***both GTX112 and GTX116***. A PRBS generator is available to drive a programmable data sequence out any SERDES link. A matching PRBS receiver will lock on to the pattern and compare received data to transmitted data for bit-error-rate-testing (BERT).

REGISTER 0x0005: NUMBER OF COMMAS AFTER RESET

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	INITIAL NUMBER OF COMMAS AFTER RESET															

GENERAL USAGE

Change as desired. Refer to the **Understanding the PRBS data sequence** section on page 26.

DEFAULT VALUE AT POWER UP : 0x0020.

REGISTER 0x0006: NUMBER OF WORDS TO SEND BEFORE INSERTING COMMA(S)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Number of words to send before inserting comma character(s)															

GENERAL USAGE

Change as desired. Refer to the **Understanding the PRBS data sequence** section on page 26.

DEFAULT VALUE AT POWER UP : 0x0040.

REGISTER 0x0007: NUMBER OF COMMAS TO SEND IN COMMA BREAKS

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RW	UNUSED	# of commas

GENERAL USAGE

Change as desired. Refer to the **Understanding the PRBS data sequence** section on page 26.

DEFAULT VALUE AT POWER UP : 0x0002.

REGISTER 0x0008: TOTAL NON-COMMA PATTERN LENGTH BEFORE PATTERN RESTART

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Number of words to send before restarting PRBS sequence.															

GENERAL USAGE

Change as desired. Refer to the **Understanding the PRBS data sequence** section on page 26.

DEFAULT VALUE AT POWER UP : 0x0100.

SSB EMULATOR: ADDRESS 009 : UNUSED

This register is unused and reserved for future expansion.

SSB EMULATOR: ADDRESS 00A : UNUSED

This register is unused and reserved for future expansion.

SSB EMULATOR: ADDRESS 00B : ILA_MUX_CTL_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	DDR ILA MUX SEL		GTX 116 TX/RX ILA MUX SEL		GTX 115 TX/RX ILA MUX SEL		GTX 114 TX/RX ILA MUX SEL		GTX 113 TX/RX ILA MUX SEL		GTX 112 TX ILA MUX SEL	

BIT DEFINITIONS

- The GTX MUX SEL bits select which of the four SERDES links in the GTX quad is sampled for the GTX ILA. The order and format of the ILA doesn't change, just which SERDES is being monitored.
  - For GTX 112, 00:X0Y0, 01:X0Y1, 10:X0Y2, 11:X0Y3. Same relative order for other GTX quads.
  - For GTX 112 and 116, only the TX-side ILA is multiplexed. For GTX 113, 114 & 115, the mux selection is common to both the TX-side and RX-side ILAs.
- Similarly the DDR MUX SEL bits select which emulator instantiation is to be monitored.

GENERAL USAGE

The Emulator firmware implements a number of Chipscope© internal logic analyzer blocks. The bit-pairs in this register allow the user to configure which of the four links for each GTX block is being monitored.

DEFAULT VALUE AT POWER UP

0x0000.

SSB EMULATOR: ADDRESSES 00C, 00D, 00E, 00F : TX_SEED REGISTERS

These registers define the starting (seed) value to use in the PRBS generators (frame generators). The register at address 0x00C defines the seed for link 0 of all GTX instances; register D controls lane 1 of all GTX, etc.. TX_SEED0 defaults at power-up to 0x0135; TX_SEED1 to 0x1234, TX_SEED2 to 0x5678 and TX_SEED3 to 0xF18A.

SSB EMULATOR: ADDRESSES 010, 011, 012, 013 : FIFO PROG THRESHOLDS

Registers 0x0010 and 0x0011 define the Programmable Empty and Programmable Full thresholds of the SFP input FIFOs. Similarly, registers 0x0012 and 0x0013 define the Programmable Empty and Programmable Full for the RTM output FIFOs.

SSB EMULATOR : ADDRESSES 014, 015, 016, 017 : NUMBER OF RECORDS REGISTERS

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	NUMBER OF RECORDS TO SEND															

GENERAL USAGE

These registers control the operation of the Core Crate Emulator logic in the U2 firmware. There are four registers, one per SERDES link in the Quad. The GTX112 Quad and the GTX116 Quad are both tied to these registers so that link #n of GTX112 will be set the same as link #n of GTX116. The sixteen-bit value written to these records is loaded into a counter to determine the number of records that is sent in response to enabling the emulator logic. The number of records that will be sent is equal to the value in the register, plus one. That is, a value of zero sends one record.

DEFAULT VALUE AT POWER UP

0x0000.

SSB EMULATOR : ADDRESSES 018, 019, 01A, 01B : RECORD DELAY REGISTERS

These registers control the operation of the Core Crate Emulator logic in the U2 firmware. There are four registers, one per SERDES link in the Quad. The GTX112 Quad and the GTX116 Quad are both tied to these registers so that link #n of GTX112 will be set the same as link #n of GTX116.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	FIX/ RND	RAND RANGE			MINIMUM FIXED DELAY											

BIT DEFINITIONS

- Bit 15 selects whether the delay time between records will be fixed (bit SET) or pseudo-random (bit CLEAR)
    - In the FIXED mode (bit 15 set), the delay time between records is determined by the value of bits 11:0 and bits 14:12 are ignored.
    - In the RANDOM mode (bit 15 clear), the delay time between records is a bounded pseudo-random number, selected by the RAND RANGE (bits 14:12) and MINIMUM FIXED DELAY (bits 11:0) fields.
        - The RAND RANGE field selects one of eight ranges:

- If bits 14:12 are “000”, the random mode degrades to a fixed number of clock ticks of delay, defined by the MINIMUM FIXED DELAY.
- Settings from “001” through “111” select a power-of-two range of a random value that is added to the MINIMUM FIXED DELAY value so that the number of tracks will range as follows.
- “001” : Either MINIMUM FIXED DELAY or (MINIMUM FIXED DELAY + 1)
- “010” : between MINIMUM FIXED DELAY and (MINIMUM FIXED DELAY + 3)
- “011” : between MINIMUM FIXED DELAY and (MINIMUM FIXED DELAY + 7)
- “100” : between MINIMUM FIXED DELAY and (MINIMUM FIXED DELAY + 15)
- “101” : between MINIMUM FIXED DELAY and (MINIMUM FIXED DELAY + 31)
- “110” : between MINIMUM FIXED DELAY and (MINIMUM FIXED DELAY + 63)
- “111” : between MINIMUM FIXED DELAY and (MINIMUM FIXED DELAY + 127)

GENERAL USAGE

These registers define the inter-record timing characteristics of the emulator firmware. Control of the number of tracks per record is in a separate set of registers. Delay times are always expressed as a number of clock ticks of the GTX TX clock (normally, 1 tick = 10ns as the TX clock is 100MHz).

DEFAULT VALUE AT POWER UP

0x8010. This results in a fixed delay of 16 clock ticks, or 160ns, between records.

SSB EMULATOR U2 : ADDRESS 01C : RESERVED

This register is reserved for engineering diagnostics use.

SSB EMULATOR: ADDRESS 01D : CORE_CRATE_STATUS_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	CORE CRATE STATUS VALUE															

GENERAL USAGE

This register defines the data value that is sent by the Core Crate Emulation logic as the 8th word in the Record Trailer. It may be loaded with any arbitrary value the user desires.

DEFAULT VALUE AT POWER UP

0xDDDD.

SSB EMULATOR: ADDRESS 01E : CORE_CRATE_ERROR_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	CORE CRATE ERROR VALUE															

GENERAL USAGE

This register defines the data value that is sent by the Core Crate Emulation logic as the 7th word in the Record Trailer. It may be loaded with any arbitrary value the user desires.

DEFAULT VALUE AT POWER UP

0xEEEE.

SSB EMULATOR: ADDRESS 01F : CORE_CRATE_CONTROL_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	SEND LONG L1ID				SEND FOREVER				RESET PRBS MACHINE				ENABLE PRBS DATA			

GENERAL USAGE

This register controls the overall operation of the Core Crate Emulator and PRBS logic in the Emulator firmware. Additional control is located in the CORE_CRATE_AUX_CTL register at address 0x02D.

BIT DEFINITIONS

- Bits 3:0, if set, select PRBS test data as the data that the Emulator will send out the fiber optic links. Each bit is associated with one of the four SFP links of GTX 112 (0 to 0, 1 to 1, etc.). If clear, FTK emulation data is selected.
- Bits 7:4, in the same SERDES order as bits 3:0, hold the PRBS logic in reset when set, resulting in continuous transmission of the K28.5 comma word.
- Bits 11:8, in the same SERDES order as bits 3:0, tell the CoreCrateEmulator logic to ignore the NUMBER_OF_RECORDS registers and send FTK emulation data forever. Upon clearing these "send forever" bits, the sending of data will stop after no more than the NUMBER_OF_RECORDS of additional records are sent.
- Bits 15:12 select whether the Emulator logic will send short (24-bit) or long (32 bit) Level 1 ID values.
    - If the SEND LONG L1 ID bit is *CLEAR*, the emulator sends bits 23:0 of the internally calculated USER_LEVEL_1_ID value and bits 31:24 of the Level 1 ID field are all zeroes.
    - If the SEND LONG L1 ID bit is *SET*, the emulator sends one of two long formats dependent upon the state of bit 0 of the CORE CRATE AUX CTL register at address 02D:
        - If bit 0 of the CORE CRATE AUX CTL register is *SET*, then the full 32-bit USER COUNTER value is used as the Level 1 ID.
        - If bit 0 of the CORE CRATE AUX CTL register is *CLEAR*, then the 24-bit Level 1 ID value is concatenated with an 8-bit EVENT COUNTER to form the 32-bit Level 1 ID, as is done in ATLAS.
    - The EVENT COUNTER is sensitive to the RESET_SSB_COUNTERS signal that comes from a pulsed control register. The EVENT COUNTER's response to RESET_SSB_COUNTERS is also modulated by the SEND LONG L1 ID bit:
        - If the SEND LONG L1 ID bit is *CLEAR*, the Event Counter is reset to 0x01 by RESET_SSB_COUNTERS.
        - If the SEND LONG L1 ID bit is *SET*, the Event Counter is *incremented* by RESET_SSB_COUNTERS.
        - RESET_SSB_COUNTERS also has the effect of resetting the USER LEVEL 1 ID value to zero.

DEFAULT VALUE AT POWER UP

0x0FFF.

SSB EMULATOR: ADDRESSES 020 - 023 : NUMBER_OF_TRACKS

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	FIX/ RND	RAND RANGE			RAND OFFSET				FIXED # of TRACKS							

BIT DEFINITIONS

- Bit 15 selects whether the number of tracks will be fixed (bit SET) or pseudo-random (bit CLEAR).
    - In the FIXED mode (bit 15 set), the number of tracks is determined by the value of bits 7:0 and bits 14:8 are ignored.
    - In the RANDOM mode (bit 15 clear), the number of tracks generated each event is a bounded pseudo-random number, selected by the RAND RANGE (bits 14:12) and RAND OFFSET (bits 11:8) fields.
        - The RAND RANGE field selects one of eight ranges:
        - If bits 14:12 are “000”, the random mode degrades to a fixed number of tracks, defined by the RAND OFFSET.
        - Settings from “001” through “111” select a power-of-two range of a random value that is added to the RAND OFFSET value so that the number of tracks will range as follows.
        - “001” : Either RAND OFFSET or (RAND OFFSET + 1)
        - “010” : between RAND OFFSET and (RAND OFFSET + 3)
        - “011” : between RAND OFFSET and (RAND OFFSET + 7)
        - “100” : between RAND OFFSET and (RAND OFFSET + 15)
        - “101” : between RAND OFFSET and (RAND OFFSET + 31)
        - “110” : between RAND OFFSET and (RAND OFFSET + 63)
        - “111” : between RAND OFFSET and (RAND OFFSET + 127)

GENERAL USAGE

These registers control the operation of the Core Crate Emulator logic in the SSB Emulator firmware. There are four registers, one per SERDES link in the Quad. The GTX112 Quad and the GTX116 Quad are both tied to these registers so that link #n of GTX112 will be set the same as link #n of GTX116.

DEFAULT VALUE AT POWER UP

0x8003.

SSB EMULATOR: ADDRESS 024/025/026 : GTX113/114/115_CTL_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Unused								ENABLE TIMING TAGS				ENABLE FIFO DATA			

GENERAL USAGE

These registers control the operation of the Generic_GTX blocks used to implement inter-FGPA serial links.

BIT DEFINITIONS

- Bits 3:0 control the TX multiplexer logic within each GTX block. Each bit is associated with one of the four SERDES links of the GTX Quad.
    - If the bit is *SET*, the data transmitted by the SERDES is the data available from a TX FIFO. A state machine constantly monitors the TX FIFO and when a full event is available, the TX machine reads the entire event out.

- If the bit is *CLEAR*, the data transmitted by the SERDES is PRBS test data generated by the *frame generator* logic.

- Bits 7:4, in the same SERDES order as bits 3:0, enable the automatic insertion of "timing tags" into the received data stream.
  - If the bit is *SET*, the "timing tag" (an extra FIFO bit not part of the data) is set each time the incoming data is either X"0000" or X"5A5A". A different "timing tag" bit is set for each of the two data values.
  - These two "timing tag" bits are connected to the Chipscope RX-side of the Generic_GTX logic and may be used to easily trigger the capture of received data.
  - A value of X"0000" marks the start of a PRBS data pattern. A value of X"5A5A" is one of the values used in the Record Trailer of SSB data for synchronization.

SSB EMULATOR: ADDRESS 027 : FIXED_L1A_VALUE

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	User defined Level 1 Accept (L1A) value															

GENERAL USAGE

The Emulation logic implements a variety of programmable "error on demand" controls to allow the simulation of a variety of problems. One of these is the REQUEST_FIXED_L1A control. When the REQUEST_FIXED_L1A is set, the Level 1 Accept value issued for the event will be the value of this register instead of the next ordinal counter value.

DEFAULT VALUE AT POWER UP

0x0000.

SSB EMULATOR: ADDRESS 028 : DIAG_BLOCK_SIZE

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	Number of words to send in diagnostic block							

GENERAL USAGE

The data format as of version 1.7.2 defines a *diagnostic data block* in the Record Trailer of each event. The diagnostic data block begins with the first words of the Record Trailer and has a fixed value of 0xE0DA, followed by the # of words of diagnostic data. If the number is zero the next word expected is 0xE0DF (marker for end of diagnostic data), followed by a 2nd copy of the diagnostic block length.

Within the Emulator state machine, a control bit REQUEST_DIAG_BLOCK can be set prior to the transmission of any event. If REQUEST_DIAG_BLOCK is sent, the value of this register replaces the normal value of zero for the # of words of diagnostic data. The "diagnostic data" sent by the Emulator is the value 0xDDnn in each word, where "nn" is a simple counter that counts down from the # of words requested to 0.

The SSB Emulator firmware generates 16-bit data words to match the output of the SSB. However, on the S-Link side of the FLIC all data is 32-bit words. The DIAG_BLOCK_SIZE is the number of 16-bit words of diagnostic data to send, but only bits 7:1 are used to enforce only even numbers.

DEFAULT VALUE AT POWER UP

0x0000.

SSB EMULATOR: ADDRESS 029 – 02C : (RESERVED)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	FIFO Programmable threshold															

GENERAL USAGE

These currently non-functional register addresses are reserved for the future implementation of programmable FULL and programmable EMPTY thresholds in the RX-side FIFOs of inter-FPGA links.

SSB EMULATOR : ADDRESS 02D : CORE_CRATE_AUX_CTL

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Link=>	**Link 3**				**Link 2**				**Link 1**				**Link 0**			
RW	LONG L1 ID MODE	ERR SEL	RST DOM X LATCH	EN PAUSE	LONG L1 ID MODE	ERR SEL	RST DOM X LATCH	EN PAUSE	LONG L1 ID MODE	ERR SEL	RST DOM X LATCH	EN PAUSE	LONG L1 ID MODE	ERR SEL	RST DOM X LATCH	EN PAUSE

GENERAL USAGE

This register is implemented as four "fields", one per SERDES link, with the same arrangement of bits in each "field".

BIT DEFINITIONS

- The LONG_L1_ID_MODE bits work in concert with the SEND_LONG_L1_ID bits found in the CORE_CRATE_CTL register (address 0x1F). If the SEND_LONG_L1_ID bit is set, one of two forms of a long (32-bit) Level 1 ID are supported as selected by the LONG_L1_ID_MODE bit in this register:
  - If LONG_L1_ID_MODE is **set**, the L1 ID issued by the emulator is a simple 32-bit counter.
  - If LONG_L1_ID_MODE is **clear**, the L1 ID issued by the emulator is an eight-bit *event counter* in bits 31:24 and a 24-bit L1 counter in bits 23:0. This is the standard ROS mode.
- The ERR SEL bits select the *source* of user-defined errors:
  - If the ERR SEL bit is **set**, the various error types are initiated by the *Error Inject RAMs* defined later in this document. These RAMs are indexed by a counter that increments each *Record*, and the counter is reset by the FRAME_GEN reset of the given GTX block. The *Error Inject RAMs* provide a facility to load a list of which errors (if any) the user wants the emulator to generate on a record-by-record basis.
  - If the ERR SEL bit is **clear**, the various error types are initiated manually by writes to the *Request Emulator Error* pulsed-control register for the given GTX.
- The RST DOM X LATCH bits, if set, hold the domain-crossing latches for the *Request Emulator Error* pulsed control signals reset, blocking the effect of the *Request Emulator Error* registers. Normally these resets are asserted once after initializing the emulator to ensure correct operation and then not used again.
- The EN PAUSE bits, if set, allow the emulator state machine to respond to flow control messages from the Processor FPGAs over the SERDES link. If these bits are clear the Emulator will ignore flow control messages, allowing the Emulator to overrun the pipeline logic. Normally these bits should be set, but they may be cleared for specific firmware tests.
  - Enabling response to flow control *only* enables response to bit 0 of the flow control messages (XON/XOFF) from the Processor FPGA. No other status/control bits from the processor FPGA are monitored.

DEFAULT VALUE AT POWER UP

0x3333. This defaults to all links honoring flow control and with the domain crossing latches held reset.

SSB EMULATOR: ADDRESS 02E : COUNTER_CTL

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	GTX 113		GTX 114		GTX 115		NA	NA	NA	NA	NA	NA
RW	X	X	X	X	CNT RESET	CNT MODE	CNT RESET	CNT MODE	CNT RESET	CNT MODE	X	X	X	X	X	X

BIT DEFINITIONS

- CNT RESET bits hold the various counters (REFCLK, TXCLK, RXCLK) inside the Generic_GTX block reset.
- CNT MODE bits set the various counters inside a Generic_GTX block into RATE mode (bit SET) or COUNT mode (bit CLEAR).

DEFAULT VALUE AT POWER UP

0x0000.

SSB EMULATOR: ADDRESS 02F/20F : HELD_RESETS / PULSED_RESETS

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
RW	X	X	TX MACH RST	X	X	X	TX FIFO RST	X	X	X	X	X	X	X	X	X

BIT DEFINITIONS

The value of the HELD_RESETS register is bit-by-bit ORed with the value written to the PULSED_RESETS register to create the SUBSECTION_RESETS bit vector within the code. The intent (only partially realized as of August 4, 2015) is to provide a mechanism akin to that previously implemented for GTX112 and GTX116 implementations in which the user may either hold reset or momentarily reset various Generic_GTX functions. The intention was to provide four bits per GTX block:

- TX FIFO reset
- TX machine reset
- RX FIFO reset
- RX machine reset

However, this has not been realized. As of the current writing (8/4/15) only bits 9 and 13 do anything. Bit 9 is the TX FIFO reset that applies to all of GTX113, GTX114 and GTX115 identically, and bit 13 is a TX machine reset that applies to all of GTX113, GTX114 and GTX115.

Future revisions of the code will revisit these registers.

DEFAULT VALUE AT POWER UP

0x0000.

SSB EMULATOR: ADDRESS 080 - 087 : USER DATA FIFOs

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Arbitrary User Data															

GENERAL USAGE

The Emulator state machines have the option of storing user-defined data that may be sent in lieu of state machine generated data. Each FIFO buffer is 8192 elements long and 16 bits wide. Addresses 0x080 through 0x083 are the FIFOs for links 0,1,2,3 of GTX112 (front SFP) and addresses 0x84 – 0x87 are for GTX116 (RTM). Each FIFO is *write only* from the PIC (Ethernet) port; once loaded the FIFOs are emptied by the emulator state machines when ENABLE_FIFO_DATA bit from the appropriate pulsed control register is set.

SSB EMULATOR U2: ADDRESS 100 : CODE_REVISION

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Major Revision				Minor Revision				Sub-Revision				Day Index			

GENERAL USAGE

The CODE_REVISION register provides a location to read the current version of the FLIC firmware. This register is changed when the firmware is modified to allow the user to determine if the board contains the latest revision of firmware. The current value as of November 6, 2014 is 0x0105 (Version 0.1.0.5).

SSB EMULATOR U2: ADDRESS 101 : CODE_DATE_YYYY

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Year of last code revision															

GENERAL USAGE

The CODE_DATE_YYYY register provides a location to read the date, as stored by the firmware engineer, of the version of code within the FPGA.

SSB EMULATOR U2: ADDRESS 101 : CODE_DATE_MMDD

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Month of last code revision								Day of month of last code revision							

GENERAL USAGE

The CODE_DATE_MMDD register provides a location to read the date, as stored by the firmware engineer, of the version of code within the FPGA.

SSB EMULATOR U2 : ADDRESS 103 : SFP_STATUS_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	LOS				MOD_PRESENT				RATESEL				TFAULT			

BIT DEFINITIONS

- The LOS (Loss Of Signal) field reads back the loss of signal indicator from each of SFP0 through SFP3 (bit 12: SFP0, 13:1, 14:2, 15:3). The LOS bit is set if the receiving optics of the given SFP fails to detect an optical signal.

- The MOD_PRESENT lines are pulled up by resistors on the FLIC but pulled down by the SFP module when the module is inserted; thus 0 is “module present” and 1 is “module absent”.

- The RATESEL bits are reserved for identification of multi-speed transceivers.

- The TFAULT bits, if high, indicate a transmitter fault. TFAULT is an open-collector signal requiring a pullup resistor on the FLIC to operate.

SSB EMULATOR U2 : ADDRESS 104 : RTM_SFP_STATUS_REG

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	LOS				MOD_PRESENT				RATESEL				0	0	0	0

SSB EMULATOR U2 : ADDRESSES 105 - 108 : GTX112 USER RUN NUMBER

These registers read back the User Run Number counter from each Core Crate Emulator in GTX112.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	User Run Number															

The Core Crate Emulator code implements a User Run Number that is part of the SSB data. As of 20150605, a fixed value of 0x12345678 is used as the ROBIN has problems with the run number incrementing. When/if an incrementing or user-programmable User Run Number is added to the firmware, these four registers will read the current value of the User Run Number.

SSB EMULATOR U2 : ADDRESSES 109 – 10C : GTX112 Level 1 ID

These registers read back the lower 16 bits of the Level 1 ID counter from each Core Crate Emulator in GTX112.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	User Level 1 ID															

The Core Crate Emulator code implements a 32-bit Level 1 ID value that can take various forms depending upon various control bits, but is in general a counter that increments each record. The user may read the lower 16 bits of the Level 1 ID value from each Core Crate Emulation block of GTX112 in these registers.

SSB EMULATOR U2 : ADDRESS 10D : GTX112 Status

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Link 3				Link 2				Link 1				Link 0			
RO	RX BYTE ALIGN	COMMA	RX RESET DONE	TX RESET DONE	RX BYTE ALIGN	COMMA	RX RESET DONE	TX RESET DONE	RX BYTE ALIGN	COMMA	RX RESET DONE	TX RESET DONE	RX BYTE ALIGN	COMMA	RX RESET DONE	TX RESET DONE

GENERAL USAGE

This register is implemented as four “fields”, one per SERDES link, with the same arrangement of bits in each “field”.

BIT DEFINITIONS

- The RX BYTE ALIGN bit is set if the GTX core is asserting RXBYTEISALIGNED. This indicates that the 8b/10b decoder has figured out where byte boundaries are and thus data should be valid.
- The COMMA bit is set if the GTX channel is currently sending comma characters.
- The RX RESET DONE bit is set if the GTX core has completed a reset of the receiver side. This bit is normally on all the time, but may clear temporarily when a reset occurs. If the MGTREFCLK of the GTX has failed or is running at an out-of-tolerance frequency, this bit may stick low.
- The TX RESET DONE bit is set if the GTX core has completed a reset of the transmitter side. This bit is normally on all the time, but may clear temporarily when a reset occurs. If the MGTREFCLK of the GTX has failed or is running at an out-of-tolerance frequency, this bit may stick low.

SSB EMULATOR U2 : ADDRESSES 10E, 114, 11E, 11F : GTX116 Error Counters

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	PRBS test mode error count															

GENERAL USAGE

When the GTX116 (RTM side) links are configured in the PRBS test mode, these registers count the number of PRBS errors seen. If the links are configured for data transmission, the values in these registers may change but are meaningless. The count is only valid when in PRBS test mode.

IMPORTANT NOTES

These four registers are implemented one per SERDES link, but are not at adjacent addresses.

SSB EMULATOR U2 : ADDRESS 10F : GTX112 MONITOR FIFO

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Reserved for future diagnostics															

This register is currently unused and reserved for engineering diagnostics associated with GTX112 (front side SFPs).

SSB EMULATOR U2 : ADDRESSES 110 - 113 : GTX112 Error Counters

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	PRBS test mode error count															

GENERAL USAGE

When the GTX112 (front side) links are configured in the PRBS test mode, these registers count the number of PRBS errors seen. If the links are configured for data transmission, the values in these registers may change but are meaningless. The count is only valid when in PRBS test mode.

SSB EMULATOR U2 : ADDRESSES 115 - 118 : GTX116 USER RUN NUMBER

These registers read back the User Run Number counter from each Core Crate Emulator in GTX116.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	User Run Number															

The Core Crate Emulator code implements a User Run Number that is part of the SSB data. As of 20150605, a fixed value of 0x12345678 is used as the ROBIN has problems with the run number

incrementing. When/if an incrementing or user-programmable User Run Number is added to the firmware, these four registers will read the current value of the User Run Number.

SSB EMULATOR U2 : ADDRESSES 119 – 11C : GTX116 Level 1 ID

These registers read back the lower 16 bits of the Level 1 ID counter from each Core Crate Emulator in GTX116.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	User Level 1 ID															

The Core Crate Emulator code implements a 32-bit Level 1 ID value that can take various forms depending upon various control bits, but is in general a counter that increments each record. The user may read the lower 16 bits of the Level 1 ID value from each Core Crate Emulation block of GTX116 in these registers.

SSB EMULATOR U2 : ADDRESS 11D : GTX116 Status

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Link 3				Link 2				Link 1				Link 0			
RO	RX BYTE ALIGN	COMMA	RX RESET DONE	TX RESET DONE	RX BYTE ALIGN	COMMA	RX RESET DONE	TX RESET DONE	RX BYTE ALIGN	COMMA	RX RESET DONE	TX RESET DONE	RX BYTE ALIGN	COMMA	RX RESET DONE	TX RESET DONE

GENERAL USAGE

This register is implemented as four "fields", one per SERDES link, with the same arrangement of bits in each "field".

BIT DEFINITIONS

- The RX BYTE ALIGN bit is set if the GTX core is asserting RXBYTEISALIGNED. This indicates that the 8b/10b decoder has figured out where byte boundaries are and thus data should be valid.
- The COMMA bit is set if the GTX channel is currently sending comma characters.
- The RX RESET DONE bit is set if the GTX core has completed a reset of the receiver side. This bit is normally on all the time, but may clear temporarily when a reset occurs. If the MGTREFCLK of the GTX has failed or is running at an out-of-tolerance frequency, this bit may stick low.
- The TX RESET DONE bit is set if the GTX core has completed a reset of the transmitter side. This bit is normally on all the time, but may clear temporarily when a reset occurs. If the MGTREFCLK of the GTX has failed or is running at an out-of-tolerance frequency, this bit may stick low.

SSB EMULATOR U2 : ADDRESSES 120, 124, 128 : GTX113 Clock Counters

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Free running counter															

Each of these registers implements a free-running counter driven by the REFCLK, TXCLK and RXCLK, respectively, for GTX block 113. Repeated reads may be used to verify that each clock is running.

SSB EMULATOR U2 : ADDRESSES 130, 134, 138 : GTX114 Clock Counters

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Free running counter															

Each of these registers implements a free-running counter driven by the REFCLK, TXCLK and RXCLK, respectively, for GTX block 114. Repeated reads may be used to verify that each clock is running.

SSB EMULATOR U2 : ADDRESSES 140, 144, 148 : GTX115 Clock Counters

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	Free running counter															

Each of these registers implements a free-running counter driven by the REFCLK, TXCLK and RXCLK, respectively, for GTX block 115. Repeated reads may be used to verify that each clock is running.

SSB EMULATOR U2 : ADDRESS 200 : PULSED_CTL_REG_200

Controls GTX 112 front panel SFP links.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y3				GTX X0Y2				GTX X0Y1				GTX X0Y0			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX112_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX112_RXRESET_DONE occurring some time later.

SSB EMULATOR U2 : ADDRESS 201 : PULSED_CTL_REG_201

Controls GTX 112.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	Enable SSB Data(3:0)				Enable FIFO Data(3:0)				FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- Bits 11:8 cause the Core Crate Emulators to send the contents of a user filled FIFO as SSB record data. It is assumed the records were properly formatted by the software that filled the FIFO.
- Bits 15:12 cause the Core Crate Emulators to generate a series of SSB Records using various counters, PRBS data, and the contents of the Number of Records and Record Delay registers.

SSB EMULATOR U2 : ADDRESS 202 : PULSED_CTL_REG_202

Reserved for controlling GTX 113 links; mapped identically to Address 200.

SSB EMULATOR U2 : ADDRESS 203 : PULSED_CTL_REG_203

Reserved for controlling GTX 113 features; mapped identically to Address 201.

SSB EMULATOR U2 : ADDRESS 204 : PULSED_CTL_REG_204

Reserved for controlling GTX 114 links; mapped identically to Address 200.

SSB EMULATOR U2 : ADDRESS 205 : PULSED_CTL_REG_205

Reserved for controlling GTX 114 features; mapped identically to Address 201.

SSB EMULATOR U2 : ADDRESS 206 : PULSED_CTL_REG_206

Reserved for controlling GTX 115 links; mapped identically to Address 200.

SSB EMULATOR U2 : ADDRESS 207 : PULSED_CTL_REG_207

Reserved for controlling GTX 115 features; mapped identically to Address 201.

SSB EMULATOR U2 : ADDRESS 208 : PULSED_CTL_REG_208

Controls GTX116 (RTM)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y19				GTX X0Y18				GTX X0Y17				GTX X0Y16			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX116_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX116_RXRESET_DONE occurring some time later.

SSB EMULATOR U2 : ADDRESS 209 : PULSED_CTL_REG_209

Controls GTX116 (RTM)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	X	X	X	X	X	X	X	X	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.

SSB EMULATOR U2 : ADDRESS 20A,20B,20C,20D,20E,20F : UNUSED

DEFAULT VALUE AT POWER-UP : 0x0000.

SSB EMULATOR: ADDRESS 20A,20B,20C,20D : GTX112 ERROR REQUESTS

SSB EMULATOR: ADDRESS 210,211,212,213 : GTX116 ERROR REQUESTS

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO	X	X	X	X	X	X	X	REQ DIAG BLK	REQ NO TRACK	REQ FIXED L1A	REQ TRLR ERR	REQ LYR ERR	REQ TRK ERR	REQ L1A SKIP	REQ L1A ERR	REQ HDR ERR

BIT DEFINITIONS

Each bit in these pulsed control registers requests that an error of the specific type be generated in the next set of machine-generated data. Four of these registers request errors for the four front panel (GTX112) data emulators and four request errors in the RTM (GTX116) data emulators. A request, once placed, is latched until the state machine loops around and is able to process the error, at which point it clears. The bits, in general, may be set in any combination desired, although some bits may take priority over others. The specific definitions are

- Bit 0 is the REQUEST HEADER ERROR bit. If set, this will cause the first word of the Record Header to be sent as the value 0xBAD1, rather than the usual 0xB0F0.
- Bit 1 is the REQUEST L1A ERROR bit. Setting this bit causes the next Level 1 Accept value to be incorrect. The exact functioning of this bit is dependent upon whether short or long L1 ID values are being sent, and whether the long L1 ID mode is set or clear. A table best describes the options.

SEND_LONG_L1_ID	LONG_L1_ID_MODE	Erroneous value upon request
0	X	The lower 16 bits of the L1 Id will be sent inverted.
1	0	Bits 31:0 of the L1 ID will be sent inverted.
1	1	Bits 23:0 of the L1 ID will be sent inverted.

    - The REQUEST L1A ERROR bit takes precedence over the REQUEST FIXED L1A bit.
- Bit 2 is the REQUEST L1A SKIP bit. If set, the internal counter used to generate the L1 ID value will increment by 2 instead of 1 at the next event.
- Bit 3 is the REQUEST TRACK ERROR bit. If set, the lower 12 bits of the Track Header data will be 0xBAD, rather than the normal 0xBDA.
- Bit 4 is the REQUEST LAYER ERROR bit. If set, the emulator will generate an event with 11 layers of data rather than the normal 12 layers. The IBL layer will be skipped.
- Bit 5 is the REQUEST TRAILER ERROR bit. If set, the emulator will issue the value 0xEBAD as the first word of the Record Trailer instead of the correct value of 0xE0DA.
- Bit 6 is the REQUEST FIXED L1A bit. If set, and if bit 1 is also clear, the emulator will send a fixed Level 1 Accept value taken from a register rather than the value of the internal counter.

- Bit 7 is the REQUEST NO TRACKS bit. If set, the emulator will skip directly from the last word of the Record Header to the first word of the Record Trailer, and issue no track data.
- Bit 8 is the REQUEST DIAG BLOCK bit. If set, the emulator will insert a diagnostic block into the next event whose length is determined by the value in the DIAG BLOCK SIZE register (address 0x02D).
- Bits 15:9 are currently unassigned and have no effect.

Format of Register as compared Emulator Error RAMs

The format of the data values written to the Emulator Error RAM buffers is exactly the same as the format for the Error Request register.

FLIC FPGA U3 (Data Collector)

In the final implementation of the FLIC FPGAs U3 and U4 act as data collector objects, receiving the data streams from U1 and U2, merging event fragments and sending those merged fragments to processor blades in the ATCA shelf for monitoring or alternate triggering purposes. A second function of FPGA U3 is the control of the reference clock chip that is used by FPGAs U1 and U2 for the front panel SFP links.

FPGA U3: ADDRESS 000 : SFP_CLOCK_CONTROL_REG

For U3, the SFP_Clock Control register controls the pins of the clock generator that provides the reference clock for all front panel SFP SERDES links in both U1 and U2.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	PR1	PR0	X	OD2	OD1	OD0	X	X	OS1	OS0	X	X	RST	CE

This register sets the operational parameters of the clock generator chip. We have a 25MHz crystal. Selections that make sense for a 25MHz input are as follows. The nominal FLIC settings are highlighted (orange for 2Gbps, green for 3Gbps).

Fin(MHz)	Feedback	Prescale	PR1/0	VCO	Odiv	Fout	ExpectedUse
25	15	5	01	1875	8(111)	46.875	
25	15	5	01	1875	6(101)	62.5	1Gbps_raw_8b/10b
25	20	4	11	2000	8(111)	62.5	1Gbps_raw_8b/10b
25	24	3	00	1800	8(111)	75	
25	25	3	10	1875	8(111)	78.125	
25	20	4	11	2000	6(101)	83.333	
25	15	5	01	1875	4(011)	93.75	
25	24	3	00	1800	6(101)	100	
25	25	3	10	1875	6(101)	104.167	
25	15	5	01	1875	3(010)	125	2Gbps_raw_8b/10b_(Slink_current)
25	20	4	11	2000	4(011)	125	2Gbps_raw_8b/10b_(Slink_current)
25	24	3	00	1800	4(011)	150	
25	25	3	10	1875	4(011)	156.25	10G_Ethernet_3.125Gb/s_raw_8b/10b
25	20	4	11	2000	3(010)	166.667	
25	15	5	01	1875	2(001)	187.5	3Gbps_raw_8b/10b
25	24	3	00	1800	3(010)	200	DDR_Reference_Clock
25	25	3	10	1875	3(010)	208.333	
25	20	4	11	2000	2(001)	250	4Gbps_raw_8b/10b
25	25	3	10	1875	2(001)	312.5	5Gbps_raw_8b/10b
25	15	5	01	1875	1(000)	375	Aurora_6Gbps_raw_8b/10b
25	20	4	11	2000	1(000)	500	
25	24	3	00	1800	1(000)	600	
25	25	3	10	1875	1(000)	625	

The two PR pins define the prescaler divider as well as the feedback divider. The FLIC normal setting is highlighted.

CONTROL INPUTS		PRESCALER	FEEDBACK	PFD FREQUENCY	
PR1	PR0	DIVIDER	DIVIDER	MINIMUM	MAXIMUM
0	0	3	24	24.305	28.47
0	1	5	15	23.33	27.33
1	0	3	25	23.33	27.33
1	1	4	20	21.875	25.62

The three OD pins define the output divider:

OD2	OD1	OD0	OUTPUT DIVIDER
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	Reserved
1	0	1	6
1	1	0	Reserved
1	1	1	8

The two OS pins define the output TYPE. The correct setting for all frequencies in the FLIC is LVDS.

CONTROL INPUTS			
OS1	OS0	OUTPUT TYPE	
0	0	LVCMOS	OSC_OUT Off
0	1	LVDS	OSC_OUT Off
1	0	LVPECL	OSC_OUT Off
1	1	LVPECL	OSC_OUT On

The CE (the data sheet for the clock chip refers to is as “output enable”) is active HIGH. If the CE pin is low, outputs are all high-Z. The RESET is active low. A 0->1 edge resets the PLL, then the '1' level lets the chip run. To load new parameters into the clock chip, the OD, OS and PR pins are first set up and then the RESET pin is toggled low, then back high again.

USAGE

Normally this register is left untouched. Immediately upon coming active after programming U3, a state machine first asserts CE=0, RESET=1. After 20ns, the state is changed to CE=1, RESET=0. After a delay of 5.12us, the state is finalized at CE=1, RESET=1 and the clock generator should be active. In the initial state machine setup of the clock generator, the PR, OD and OS bits are hard-coded to OD=”011” and PR=”11”, the setting for 2Gbps operation.

Procedure to manually change SFP clock frequency

Should the user wish to change the setting of the clock generator, the SFP_CLOCK_CONTROL register should first be set with the correct values in the PR, OD and OS fields, and also with both the CE and RESET bits high. For 3Gpbs operation the correct initial value is 0x1113. After setting the SFP_CLOCK_CONTROL register, the user then performs the following sequence:

1. Set bit 0 of the GENERAL_CTL register to enable manual control of the clock generator. The value of the SFP_CLOCK_CONTROL register is immediately asserted onto the clock generator pins. The default value of 0x1113 sets CE=1, RESET=1.
2. Write the SFP_CLOCK_CONTROL register with the correct value for PR, OD and OS, but set the RESET bit *low* and the CE bit *high*. (e.g., 0x1111 for 3Gbps).
3. Write the SFP_CLOCK_CONTROL register to toggle the RESET bit back high (e.g. 0x1113).
4. Finally, enable the clock generator to drive the new frequency by setting the RESET bit high and the CE bit *low* in the SFP_CLOCK_CONTROL register. (e.g., 0x1112).

DEFAULT VALUE AT POWER UP : 0x1113. This is the correct initial setting to allow the user to manually switch to 3Gbps operation.

FPGA U3: ADDRESS 001 : LED_REG

Generic diagnostic register allowing the user to play with two of the board's LEDs. Same functionality as U1 and U2, but different LEDs. U3 drives LEDs 9 and 8. LED8 is connected to a counter to make it blink just as a visual indicator that there is valid code in U3.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	X	X	LED9	X

USAGE

There is little to do with this register at present. It is provided for future expansion of LED functionality.

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 002 : GENERAL_CONTROL_REG

Generic control register allowing the user to override automatic settings.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	X	X	ETH CLK	SFP CLK

BIT DESCRIPTIONS

- Bit 0, if clear, leaves control of the external clock chip that sets the rate of U1's and U2's front panel SFP links to the startup state machine. Otherwise, if the bit is set, this enables use of the Clock Control Register for manual control of that clock generator's frequency.
- Bit 1, if clear, leaves control of the external clock chip that sets the rate of U3's and U4's Ethernet interfaces to the startup state machine. Otherwise, if the bit is set, this enables use of the Clock Control Register for manual control of that clock generator's frequency.

DEFAULT VALUE AT POWER-UP: 0x0000.

USAGE NOTES

U3 controls a clock generator that affects what goes on in both U1 and U2. It is critically important to set the SFP clock speed before attempting any form of communication with the SSB module.

FPGA U3: ADDRESS 003 : ETHERNET_CLOCK_CONTROL_REG

For U3, the ETHERNET_CLOCK_CONTROL register controls the pins of the clock generator that provides the reference clock for all ATCA Ethernet links in both U3 and U4.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	PR1	PR0	X	OD2	OD1	OD0	X	X	OS1	OS0	X	X	RST	CE

USAGE

Normally this register is left untouched. Immediately upon coming active after programming U3, a state machine first asserts CE=0, RESET=1. After 20ns, the state is changed to CE=1, RESET=0. After a delay of 5.12us, the state is finalized at CE=1, RESET=1 and the clock generator should be active. In the initial state machine setup of the clock generator, the PR, OD and OS bits are hard-coded to OD="011" and PR="10", the setting for 10GbE operation.

Procedure to manually change Ethernet clock frequency

Should the user wish to change the setting of the clock generator, the ETHERNET_CLOCK_CONTROL register should first be set with the correct values in the PR, OD and OS fields, and also with both the CE and RESET bits high. After setting the ETHERNET_CLOCK_CONTROL register, the user then performs the following sequence:

1. Set bit 1 of the GENERAL_CTL register to enable manual control of the clock generator. The value of the ETHERNET_CLOCK_CONTROL register is immediately asserted onto the clock generator pins. The default value of 0x1113 sets CE=1, RESET=1.
2. Write the ETHERNET_CLOCK_CONTROL register with the correct value for PR, OD and OS, but set the RESET bit *low* and the CE bit *high*.
3. Write the ETHERNET_CLOCK_CONTROL register to toggle the RESET bit back high
4. Finally, enable the clock generator to drive the new frequency by setting the RESET bit high and the CE bit *low* in the ETHERNET_CLOCK_CONTROL register.

DEFAULT VALUE AT POWER UP : 0x2313. This is the correct initial setting to allow the user to manually switch to 3Gbps operation.

FPGA U3: ADDRESS 004 : GTX112_CTL_REG

Enables/disables the GTX112 inter FPGAlinks between U3 and U4.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	TDIS3	TDSI2	TDIS1	TDIS0

BIT DEFINITIONS

Each TDIS (**T**ransmitter **DIS**able) bit, if set high, disables the associated front panel fiber transmitter. The order of these bits is that bit 0 is the leftmost SFP of the four connected to a given FPGA, as viewed looking into the front panel; bit 3 is the right-most.

DEFAULT VALUE AT POWER-UP : 0x0000. This ***enables*** all the SFP modules, so the user doesn't need to do anything to send or receive data. Normally there is no need to disable unused links.

FPGA U3: ADDRESS 005 : GTX113_CTL_REG

Enables/disables the GTX113 inter FPGAlinks between U3 and U2.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	TDIS3	TDSI2	TDIS1	TDIS0

BIT DEFINITIONS

Each TDIS (**T**ransmitter **DIS**able) bit, if set high, disables the associated front panel fiber transmitter. The order of these bits is that bit 0 is the leftmost SFP of the four connected to a given FPGA, as viewed looking into the front panel; bit 3 is the right-most.

DEFAULT VALUE AT POWER-UP : 0x0000. This ***enables*** all the SFP modules, so the user doesn't need to do anything to send or receive data. Normally there is no need to disable unused links.

FPGA U3: ADDRESS 006 : GTX114_CTL_REG

Enables/disables the GTX112 inter FPGAlinks between U3 and U1.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X	X	X	X	X	X	X	X	X	TDIS3	TDSI2	TDIS1	TDIS0

BIT DEFINITIONS

Each TDIS (**T**ransmitter **DIS**able) bit, if set high, disables the associated front panel fiber transmitter. The order of these bits is that bit 0 is the leftmost SFP of the four connected to a given FPGA, as viewed looking into the front panel; bit 3 is the right-most.

DEFAULT VALUE AT POWER-UP : 0x0000. This ***enables*** all the SFP modules, so the user doesn't need to do anything to send or receive data. Normally there is no need to disable unused links.

FPGA U3: ADDRESS 007 - 00A : PRBS CONTROL REGISTERS

This set of four registers defines the (Pseudo-Random Bit Sequence) PRBS control parameters. A PRBS generator is available to drive a programmable data sequence out any SERDES link. A matching PRBS receiver will lock on to the pattern and compare received data to transmitted data for bit-error-rate-testing (BERT).

REGISTER 0x0007: NUMBER OF COMMAS AFTER RESET

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	INITIAL NUMBER OF COMMAS AFTER RESET															

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0020.

REGISTER 0x0008: NUMBER OF WORDS TO SEND BEFORE INSERTING COMMA(S)

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Number of words to send before inserting comma character(s)															

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0040.

REGISTER 0x0009: NUMBER OF COMMAS TO SEND IN COMMA BREAKS

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	UNUSED												# of commas			

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0002.

REGISTER 0x000A: TOTAL NON-COMMA PATTERN LENGTH BEFORE PATTERN RESTART

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	Number of words to send before restarting PRBS sequence.															

USAGE: Change as desired.
DEFAULT VALUE AT POWER-UP : 0x0100.

The pseudo-random sequence is generated using a shift register with exclusive-or gates. In the current version of the U1 code, four PRBS generators and four PRBS receivers are connected to the four SERDES units associated with the four front panel SFP connections. The seed values for each PRBS are different, stored in registers at addresses 0x000C, 0x000D, 0x000E and 0x000F. The default seeds are 0x0135, 0x1234, 0x5678 and 0xF18A. A PRBS spreadsheet in the code repository may be used to generate the expected data stream for any seed.

FPGA U3: ADDRESS 00B : ILA_MUX_CTL_REG

Controls operation of the multiplexed latch in the GTX instantiations preceding the ILA for the GTX quad.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	X	X	X	X							GTX 114 MUX SEL		GTX 113 MUX SEL		GTX 112 MUX SEL	

BIT DEFINITIONS

- The GTX MUX SEL bits select which of the four SERDES links in the GTX quad is sampled for the GTX ILA. The order and format of the ILA doesn't change, just which SERDES is being monitored.
    - For GTX 112, 00:X0Y0, 01:X0Y1, 10:X0Y2, 11:X0Y3. Same relative order for other GTX quads.

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 010 : ETH1_XAUI_CTL_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 011 : ETH1_10GEMAC_TX_CONFIG_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 012 : ETH1_10GEMAC_TX_MTU_SIZE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 013 : ETH1_10GEMAC_RX_CONFIG_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 014 : ETH1_10GEMAC_RX_MTU_SIZE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 015 : ETH1_10GEMAC_PAUSE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 016 : ETH1_10GEMAC_CTL_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 017-019 : ETH1_FLIC_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 01A-01B : ETH1_FLIC_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 01C : ETH1_FLIC_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 01D-01F : ETH1_HOST_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 020-021 : ETH1_HOST_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 022 : ETH1_HOST_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 023-02F : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 030 : ETH2_XAUI_CTL_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 031 : ETH2_10GEMAC_TX_CONFIG_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 032 : ETH2_10GEMAC_TX_MTU_SIZE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 033 : ETH2_10GEMAC_RX_CONFIG_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 034 : ETH2_10GEMAC_RX_MTU_SIZE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 035 : ETH2_10GEMAC_PAUSE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 036 : ETH2_10GEMAC_CTL_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 037-039 : ETH2_FLIC_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 03A-03B : ETH2_FLIC_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 03C : ETH2_FLIC_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 03D-03F : ETH2_HOST_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 040-041 : ETH2_HOST_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 042 : ETH2_HOST_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3: ADDRESS 043-04F : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESSES 050, 051, 052, 053 : TX_SEED REGISTERS

These registers define the starting (seed) value to use in the PRBS generators (frame generators). The register at address 0x00C defines the seed for link 0 of GTX112 and also for link 0 of GTX116. TX_SEED0 defaults at power-up to 0x0135; TX_SEED1 to 0x1234, TX_SEED2 to 0x5678 and TX_SEED3 to 0xF18A.

FPGA U3: ADDRESSES 054, 055, 056, 057 : NUMBER OF TRACKS REGISTERS

These registers define the number of tracks that will be generated by each copy of the Core Crate Emulator in response to the transmit pulse control bit.

FPGA U3: ADDRESSES 058, 059, 05A, 05B : NUMBER OF RECORDS REGISTERS

These registers define the number of records that will be generated by each copy of the Core Crate Emulator in response to the transmit pulse control bit.

FPGA U3: ADDRESSES 05C, 05D, 05E, 05F : RECORD DELAY REGISTERS

These registers define the delay in clocks between records that will be generated by each copy of the Core Crate Emulator in response to the transmit pulse control bit.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	RND	RECORD DELAY(14:0)														

BIT DEFINITIONS

- The RND bit selects between a random or fixed delay between records. If RND is set, the delay is random. If RND is clear, the delay is fixed.:X0Y2, 11:X0Y3.
- The RECORD DELAY parameter is the fixed delay used between records when RND is clear.

FPGA U3: ADDRESSES 060-061 : FIFO112 PROG THRESHOLDS

Registers 0x0060 and 0x0061 define the Programmable Empty and Programmable Full thresholds of the GTX112 input FIFOs

FPGA U3: ADDRESSES 062-063 : FIFO113 PROG THRESHOLDS

Registers 0x0062 and 0x0063 define the Programmable Empty and Programmable Full thresholds of the GTX113 input FIFOs

FPGA U3: ADDRESSES 064-065 : FIFO114 PROG THRESHOLDS

Registers 0x0064 and 0x0065 define the Programmable Empty and Programmable Full thresholds of the GTX114 input FIFOs

FPGA U3: ADDRESS 066-06F : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 100 : SFP CLOCK GENERATOR STATUS

Read only status register displaying the current settings of the control bits to the SFP (front panel) clock generator chip.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	X	X	X	X	X	X	PR1	PR0	X	OD2	OD1	OD0	X	X	OS1	OS0

This register reads back the settings of the PR (prescale), OD (output divider) and OS (output select) pins as they are being driven to the SFP clock generator chip. Use the tables below to decode the setting. The expected settings that can be set by the user through the Clock Control register are highlighted in yellow. Note, in the Odiv column, that the division *factor* is not the same as the Odiv *setting*. The 3 bit code read back in the register is the *setting*, shown in the table as the value in parentheses.

Fin(MHz)	Feedback	Prescale	PR1/0	VCO	Odiv	Fout	ExpectedUse
25	15	5	01	1875	8(111)	46.875	
25	15	5	01	1875	6(101)	62.5	1Gbps_raw_8b/10b
25	20	4	11	2000	8(111)	62.5	1Gbps_raw_8b/10b
25	24	3	00	1800	8(111)	75	
25	25	3	10	1875	8(111)	78.125	
25	20	4	11	2000	6(101)	83.333	
25	15	5	01	1875	4(011)	93.75	
25	24	3	00	1800	6(101)	100	
25	25	3	10	1875	6(101)	104.167	
25	15	5	01	1875	3(010)	125	2Gbps_raw_8b/10b_(Slink_current)
25	20	4	11	2000	4(011)	125	2Gbps_raw_8b/10b_(Slink_current)
25	24	3	00	1800	4(011)	150	
25	25	3	10	1875	4(011)	156.25	10G_Ethernet_3.125Gb/s_raw_8b/10b
25	20	4	11	2000	3(010)	166.667	
25	15	5	01	1875	2(001)	187.5	3Gbps_raw_8b/10b
25	24	3	00	1800	3(010)	200	DDR_Reference_Clock
25	25	3	10	1875	3(010)	208.333	
25	20	4	11	2000	2(001)	250	4Gbps_raw_8b/10b
25	25	3	10	1875	2(001)	312.5	5Gbps_raw_8b/10b
25	15	5	01	1875	1(000)	375	Aurora_6Gbps_raw_8b/10b
25	20	4	11	2000	1(000)	500	
25	24	3	00	1800	1(000)	600	
25	25	3	10	1875	1(000)	625	

The two OS pins define the output TYPE. The correct setting for all frequencies in the FLIC is LVDS.

CONTROL INPUTS			
OS1	OS0	OUTPUT TYPE	
0	0	LVCMOS	OSC_OUT Off
0	1	LVDS	OSC_OUT Off
1	0	LVPECL	OSC_OUT Off
1	1	LVPECL	OSC_OUT On

FPGA U3 : ADDRESS 101-10F : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 110 : ETH1_XAUI_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 111 : ETH1_10GEMAC_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 112 : ETH1_10GEMAC_TX_STATISTICS_0_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 113 : ETH1_10GEMAC_TX_STATISTICS_1_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 114 : ETH1_10GEMAC_RX_STATISTICS_0_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 115 : ETH1_10GEMAC_RX_STATISTICS_1_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 116-118 : ETH1_RX_DEST_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 119-11A : ETH1_RX_DEST_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 11B : ETH1_RX_DEST_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 11C-11E : ETH1_RX_SRC_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 11F-120 : ETH1_RX_SRC_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 121 : ETH1_RX_SRC_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 122 : ETH1_RX_UDP_VALUE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 123 : ETH1_TX_IP_CHECKSUM_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 124 : ETH1_TX_IP_LENGTH_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 125 : ETH1_TX_IP_NUMBER_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 126-12F : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 130 : ETH2_XAUI_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 131 : ETH2_10GEMAC_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 132 : ETH2_10GEMAC_TX_STATISTICS_0_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 133 : ETH2_10GEMAC_TX_STATISTICS_1_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 134 : ETH2_10GEMAC_RX_STATISTICS_0_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 135 : ETH2_10GEMAC_RX_STATISTICS_1_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 136-138 : ETH2_RX_DEST_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 139-13A : ETH2_RX_DEST_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 13B : ETH2_RX_DEST_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 13C-13E : ETH2_RX_SRC_MAC_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 13F-140 : ETH2_RX_SRC_IP_ADDRESS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 141 : ETH2_RX_SRC_UDP_PORT_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 142 : ETH2_RX_UDP_VALUE_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 143 : ETH2_TX_IP_CHECKSUM_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 144 : ETH2_TX_IP_LENGTH_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 145 : ETH2_TX_IP_NUMBER_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 146-14F : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 150-153 : GTX112_RX_ERROR_COUNT REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 154-157 : GTX112_USER_RUN_NUMBER REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 158-15B : GTX112_USER_LEVEL_1_ID REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 15C : GTX112_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 15D-15E : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 15F : GTX112_MONITOR_FIFO_DOUT

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 160-163 : GTX113_RX_ERROR_COUNT REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 164-167 : GTX113_USER_RUN_NUMBER REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 168-16B : GTX113_USER_LEVEL_1_ID REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 16C : GTX113_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 16D-16E : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 16F : GTX113_MONITOR_FIFO_DOUT

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 170-173 : GTX114_RX_ERROR_COUNT REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 174-177 : GTX114_USER_RUN_NUMBER REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 178-17B : GTX114_USER_LEVEL_1_ID REGISTERS

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 17C : GTX114_STATUS_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 17D-17E : UNUSED

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 17F : GTX114_MONITOR_FIFO_DOUT

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 200 : PULSED_CTL_REG_200

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 201 : PULSED_CTL_REG_201

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 202 : ETH1_PULSED_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 203 : ETH2_PULSED_REG

Description

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO																

BIT DEFINITIONS

DEFAULT VALUE AT POWER-UP : 0x0000.

FPGA U3 : ADDRESS 204 : GTX112_PULSED_REG_0

Controls GTX 112 front panel SFP links.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y3				GTX X0Y2				GTX X0Y1				GTX X0Y0			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX112_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX112_RXRESET_DONE occurring some time later.

FPGA U3 : ADDRESS 205 : GTX112_PULSED_REG_1

Controls GTX 112.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	Enable SSB Data(3:0)				Enable FIFO Data(3:0)				FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.

- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- Bits 11:8 cause the Core Crate Emulators to send the contents of a user filled FIFO as SSB record data. It is assumed the records were properly formatted by the software that filled the FIFO.
- Bits 15:12 cause the Core Crate Emulators to generate a series of SSB Records using various counters, PRBS data, and the contents of the Number of Records and Record Delay registers.

FPGA U3 : ADDRESS 206 : GTX113_PULSED_REG_0

Controls GTX 113 front panel SFP links.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y3				GTX X0Y2				GTX X0Y1				GTX X0Y0			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX113_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX113_RXRESET_DONE occurring some time later.

FPGA U3 : ADDRESS 207 : GTX113_PULSED_REG_1

Controls GTX 113.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	Enable SSB Data(3:0)				Enable FIFO Data(3:0)				FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- Bits 11:8 cause the Core Crate Emulators to send the contents of a user filled FIFO as SSB record data. It is assumed the records were properly formatted by the software that filled the FIFO.
- Bits 15:12 cause the Core Crate Emulators to generate a series of SSB Records using various counters, PRBS data, and the contents of the Number of Records and Record Delay registers.

FPGA U3 : ADDRESS 208 : GTX114_PULSED_REG_0

Controls GTX 114 front panel SFP links.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GTX X0Y3				GTX X0Y2				GTX X0Y1				GTX X0Y0			
WO	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST	RX RST	RX PLL RST	TX RST	TX PLL RST

BIT DEFINITIONS

- TX PLL RST: reset the transmitter side PLL.
- TX RST: reset the transmitter logic. This will generate a local TXRESET sequence culminating in GTX114_TXRESET_DONE occurring some time later.
- RX PLL RST: reset the receiver side PLL.
- RX RST : reset the receiver logic. This will generate a local RXRESET sequence culminating in GTX114_RXRESET_DONE occurring some time later.

FPGA U3 : ADDRESS 209 : GTX114_PULSED_REG_1

Controls GTX 114.

BIT =>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NA	NA	NA	NA	NA	NA	NA	NA	GTX X0Y3		GTX X0Y2		GTX X0Y1		GTX X0Y0	
WO	Enable SSB Data(3:0)				Enable FIFO Data(3:0)				FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET	FR RESET	FG RESET

BIT DEFINITIONS

- FG RESET bits reset the FRAME GENERATE test logic that drives the pseudo-random sequence out the transmitter. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- FR RESET bits reset the FRAME RECEIVE test logic that compares the pseudo-random sequence received to that which is expected. The pulsed control only works if bit 15 of the GENERAL_CTL_REG (address 4) is set to force manual resets.
- Bits 11:8 cause the Core Crate Emulators to send the contents of a user filled FIFO as SSB record data. It is assumed the records were properly formatted by the software that filled the FIFO.
- Bits 15:12 cause the Core Crate Emulators to generate a series of SSB Records using various counters, PRBS data, and the contents of the Number of Records and Record Delay registers.