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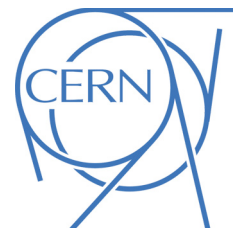
ATLAS NOTE

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A New Portable Test Bench for the Tile Calorimeter Super-Drawers

José Alves[a], Daniel Bullock[b], Fernando Carrió[c], Xin Chen[j], Jeff Dandoy[i],
Hee Yeun Kim[b], Irakli Minashvili[d], Pablo Moreno[e], Stanislav Nemecek[f],
Robert Graham Reed[e], Xifeng Ruan[e], Charles Sandrock[e], Vinícius
Schettino[g], Andrei Shalyugin[d], Carlos Solans Sanchez[h], Júlio Souza[g],
Reto Suter[e], Giulio Usai[b], Alberto Valero[c]

[a]*Laboratorio de Instrumentacao e Fisica Experimental de Particulas, Portugal*
[b]*University of Texas at Arlington, USA*
[c]*Departamento de Fisica Atómica, Molecular y Nuclear and IFIC, Spain*
[d]*Joint Institute for Nuclear Research, Dubna, Russia*
[e]*University of the Witwatersrand, Johannesburg, South Africa*
[f]*Academy of Sciences of the Czech Republic, Czech Republic*
[g]*Universidade Federal de Juiz de Fora, Brazil*
[h]*CERN*
[i]*University of Chicago, USA*
[j]*Tsinghua University, China*

Abstract

This note describes a revised version of the portable test bench that is used for the certification and quality checking of the front-end electronics of the TileCal super-drawers of the ATLAS experiment at CERN. This upgraded system modernizes the hardware as well as adding mobility to the system. It has been in use since the beginning of March 2013 for the long shutdown of the LHC, and will be used in future maintenance periods.

Contents

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1   Introduction

MobiDICK4 is an upgraded version of the stand-alone test-bench for the full certification of the front-end electronics of the Tile Calorimeter (TileCal) [1] in the ATLAS experiment [2] at CERN. This version is designed to be used in the consolidation of electronics during the long shutdown 1 of the LHC and during the future maintenance periods. The front-end Graphical User Interface (GUI) of MobiDICK4 runs on a portable computer through an Ethernet connection and communicates with the back-end server that runs on a Field Programmable Gate Array (FPGA) enabled printed circiut board. The GUI also controls several state-of-the-art daughter-boards that provide different functionalities to the motherboard. While the MobiDICK4 software keeps the client-sever architecture of previous versions, the server platform has been replaced to utilize an embedded system from the Versa Module Europa (VME) modules to modernize the hardware.

MobiDICK4 is designed to perform sixteen sets of tests on the TileCal front-end electronics, under the data taking conditions, to ensure their functionality. TileCal is a sampling calorimeter where scintillating tiles are embedded in steel absorber plates which are mechanically divided into three barrels, one central long barrel and two extended barrels. Each barrel is assembled out of 64 wedge-shaped modules staggered in the ϕ direction. On each module the tiles are grouped into cells which are read-out on both sides by a photomultiplier. The photomultiplier is located along with the rest of the front-end electronics, in what is called a super-drawer, axially oriented at the maximal radius of the barrels. The photomultiplier tubes (PMTs) convert the light into electrical pulses, which are digitized by two separate ADCs with a 1 to 64 gain ratio. These signals are also added in groups of projective towers in η by analogue summation cards and their signals are transmitted to the Level 1 Trigger through dedicated cables. Digitized data in groups of 3 PMTs are read-out by one Data Management Unit (DMU)[3]. Two DMUs are mounted on a digitizer board which is equipped with a TTCrx chip [4]. Up to eight digitizer boards read-out one super-drawer. Finally an Interface Board [5] packs and transmits the data to the back-end and receives Trigger Timing and Control (TTC) commands from it. MobiDICK4 has specific tests that target the certification of each of these components.

This document is divided into four sections. The hardware is described in Section 2, firmware to operate the hardware is described in Section 4, software to operate the tests is explained in Section 5 and the tests are described in Section 6.

2 Hardware

2.1 Motherboard

The motherboard of MobiDICK4 is a commercial Xilinx ML507 development board which implements a Virtex-5 FPGA with a real PowerPC processor embedded inside running at 400 MHz with 256 MB of DDR2 RAM. Other than the programmable logic, the FPGA populates hard-wired resources that are very useful for the test bench's purpose including a Small Form-factor Pluggable (SFP) transceiver, an ethernet port, two serial ports, a General Purpose Input/Output (GPIO) connector, a USB host and a Compact Flash memory card slot. Figure 1 is a picture of the ML507 motherboard. This is running a version of Linux in the PowerPC (Refer to Sec. 4). This development board was chosen due to the increased General Purpose I/O to allow additional boards to be added, the presence of the SFP module for better connectivity and most importantly the real PowerPC in the chip which allows the installation of a Linux Operating System.
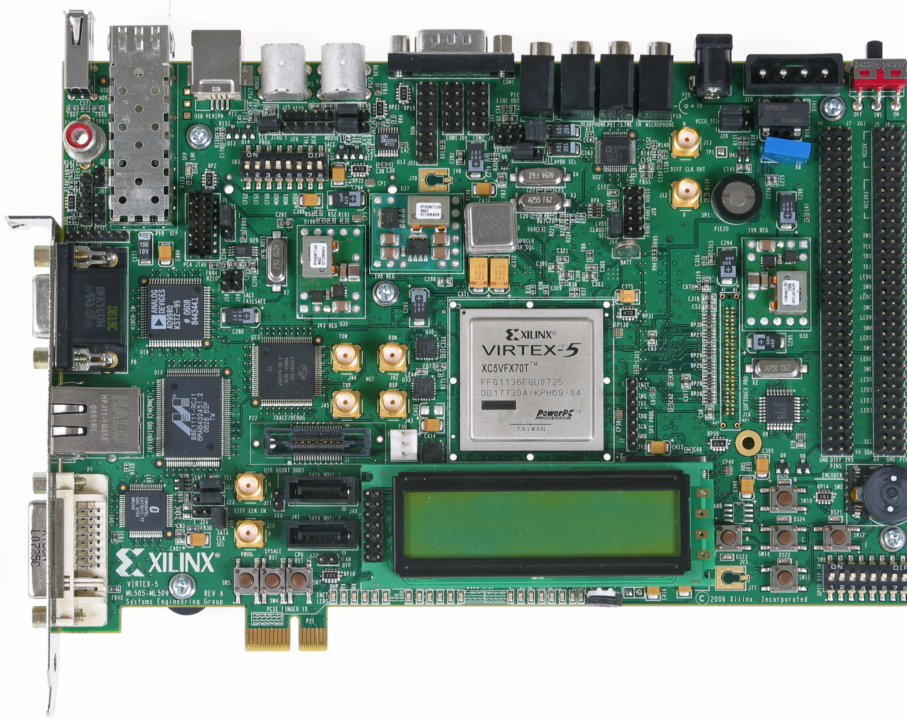
Figure 1: The ML507 motherboard

This board is available from Xilinx in the USA at the estimated cost at USD 1,500 at the time of writing. Due to the European regulations on the manufacturing process, it cannot be shipped to any European countries. There is also a donation program available.

2.2 ADC board

The analog outputs provided by the super-drawer are the analog sum of projective trigger towers and the amplified signal of the outermost radial layer (D-type cells). In order to

128 test the front-end electronics generating these analog signals, MobiDICK has to be able
129 to read them. Therefore, an analog to digital conversion is needed between the front-end
130 and the motherboard. For this purpose, a custom ADC board has been designed.
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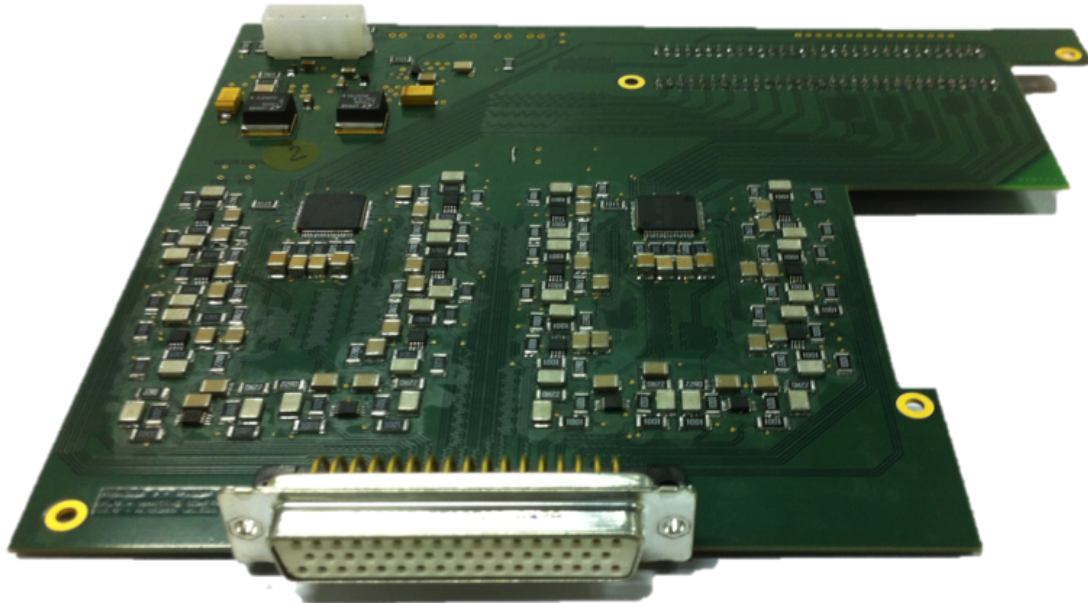
Figure 2: The ADC Board

132   The PCB holds two different ADS5271 ADC chips from Texas Instruments that sam-
133 ple the signal and transfer the collected data in series to the mother board through 32
134 differential lines. This PCB is organized in a four-layer stack-up, using the TOP and
135 BOTTOM layers to route signals in the design and a GND and a POWER layer with
136 split planes for the different supplies needed. All traces are 300 microns in width and
137 have been designed to match 50 Ohms of characteristic impedance. The lengths of all
138 channels have been equalized as much as possible.
139   A power stage comprising different regulators provide the voltages needed in the de-
sign:

LT3015	:	-3.3 V at 1.5 A	for analog negative supply
LT1529	:	+3.3 V, 3 A	for analog positive supply
TPS73633	:	+3.3 V, 400 mA	for digital supply

140
141   The analog stage includes all the components used to accommodate the muon and
142 trigger differential signals to the ADC input range. The key component here is the differ-
143 ential operational amplifier THS4151 which is set up to have a gain of 0.5 using different
144 resistor values. The operational amplifier also implements an active anti-aliasing filter
145 designed to have a cut off frequency of 20 MHz. A passive low-pass filter on the output
146 of the previous circuit adds a second pole to the system at the same frequency, setting
147 the transition from the passing band to the stop band to -40 dB/dec. Different resistors
148 implement the proper terminations at the input and the output of the analog stage. All

¹⁴⁹ the differential signals have been routed to equalize the trace lengths among the different
¹⁵⁰ channels before and after the analog stage to be sure all channels have the same delay.
¹⁵¹

¹⁵²   The digital part of the board includes the two ADS5271 chips, which are 8-channel
¹⁵³ 12-bit ADCs able to digitize up to rates of 50 MSPS, delivering serialized output streams.
¹⁵⁴ The ADC receives signals within a range of -1 V to +1 V on its differential inputs and
¹⁵⁵ samples them, providing output digital values from 0 to 4095. This particular chip has
¹⁵⁶ an SPI-based interface that allows setting the ADC into different configurations, such as
¹⁵⁷ training patterns or normal digitization, different current values in the output drivers etc.
¹⁵⁸ Patterns are used as part of the start up sequence to align the bits in the motherboard.
¹⁵⁹   The reference clock used in the digitization is provided from the motherboard, although
¹⁶⁰ a 40 MHz SMD crystal oscillator can also be mounted on board which is not recommended,
¹⁶¹ feeds a Texas Instruments CDCLVC1102 3.3 V LVCMOS high-performance clock buffer,
¹⁶² used for the proper distribution of the clock signals to the two ADCs of the board. The
¹⁶³ digitized outputs of the ADC are sent serially to the FPGA at a data rate of 480 Mbps.
¹⁶⁴ In order to be able to de-serialize these streams, the ADC sends a frame (word) clock
¹⁶⁵ and a bit clock. All these signals are differential and have been equalized among them in
¹⁶⁶ order to reach the FPGA with the smallest delay as possible.
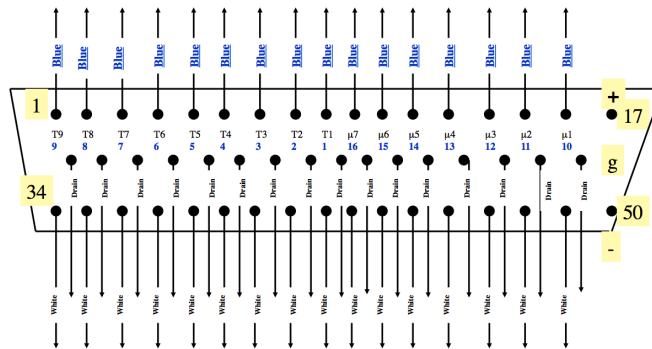
Figure 3: Schematic of Trigger Plug DB50 (Male) Barrel
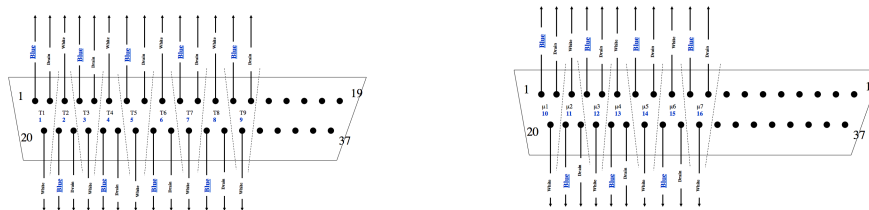
Figure 4: Pin schematics of analog signal input connectors from the drawers : Barrel
Tower Plug (left) and Barrel Muon Plug (right)

¹⁶⁷   Cabling information of the board is shown in Table 1. Figure 3 represents the SUBD-
¹⁶⁸ 50 connector's pin number match to the connected PMTs and adder numbers under
¹⁶⁹ the categories of long and extended barrels. Figure 4 shows pin matches of two cables
¹⁷⁰ receiving analog signals from the super-drawer in the same manner with the SUBD-50

171 connector. The two trigger outputs from the super-drawer (calorimeter tower and muon)
172 are connected to the patch panel of MobiDICK4 in two separate connectors. Signals from
173 both are merged into the one cable that is connected to the ADC board to be digitized.

ADC[0-15]	EBX pmt[1-48]	EBX adder[0-7]	LBX pmt[1-48]	LBX adder[0-8]
0	37	4 (muon)	26	3 (muon)
1	38	3 (muon)	15	2 (muon)
2	18	2 (muon)	14	1 (muon)
3	17	1 (muon)	1	0 (muon)
4	5,6,3,4,17	1 (tile)	1,2,3,4	0 (tile)
5	-	-	43	6 (muon)
6	-	-	40	5 (muon)
7	1	0 (muon)	27	4 (muon)
8	21,22,33,34	5 (tile)	20,21,22,23,27	4 (tile)
9	7,8,15,16,37	4 (tile)	16,17,18,19,26	3 (tile)
10	11,12,23,24,38	3 (tile)	10,11,12,13,15	2 (tile)
11	9,10,18	2 (tile)	6,7,8,9,14	1 (tile)
12	-	-	38,39,45,46,47,48	8 (tile)
13	-	-	34,37,41,42	7 (tile)
14	13,14,1,2	0 (tile)	28,31,35,36,43	6 (tile)
15	29,30,43,44,41,42	7 (tile)	24,25,29,30,40	5 (tile)

Table 1: Trigger Table

174 The ADC has 16 channels (0 through 15) and PMTs are numbered beginning from 1
175 through 48 for each long and extended barrels. There are eight adders for each extended
176 barrel and nine adders for each long barrel. One adder has both calorimeter tower and
177 muon outputs.

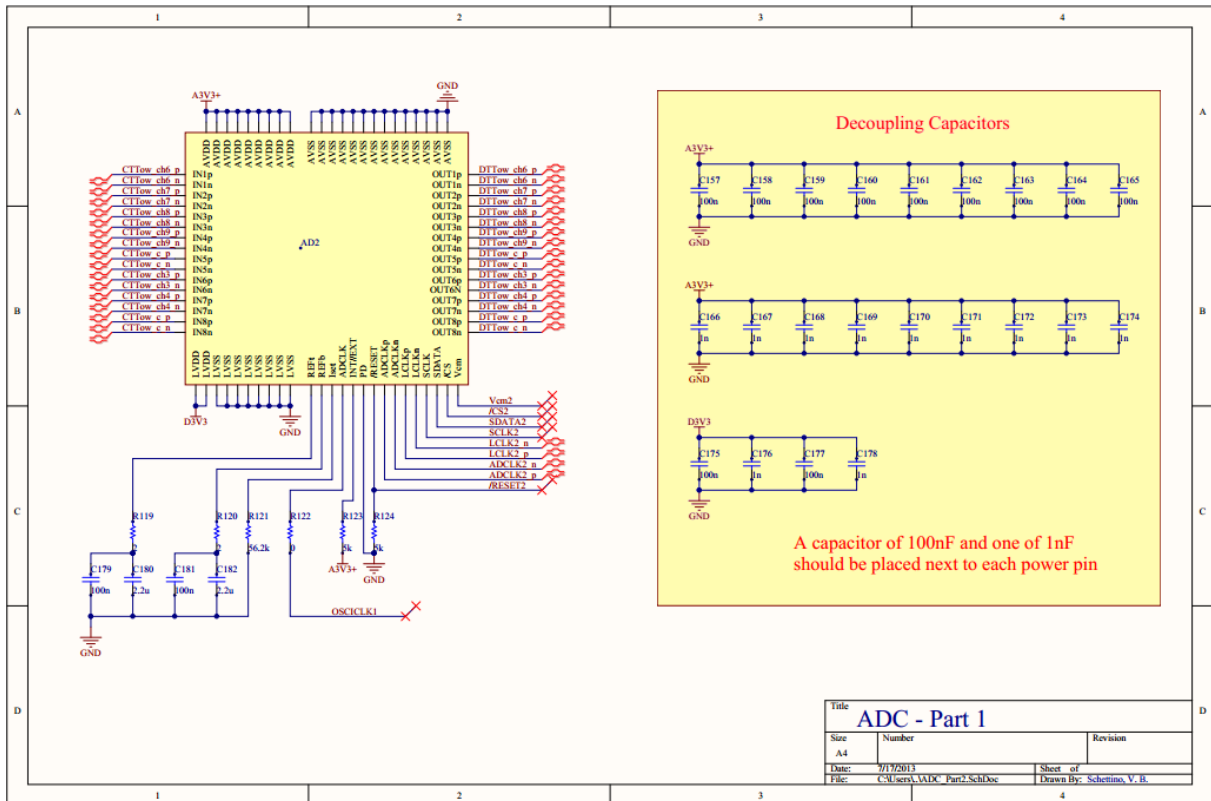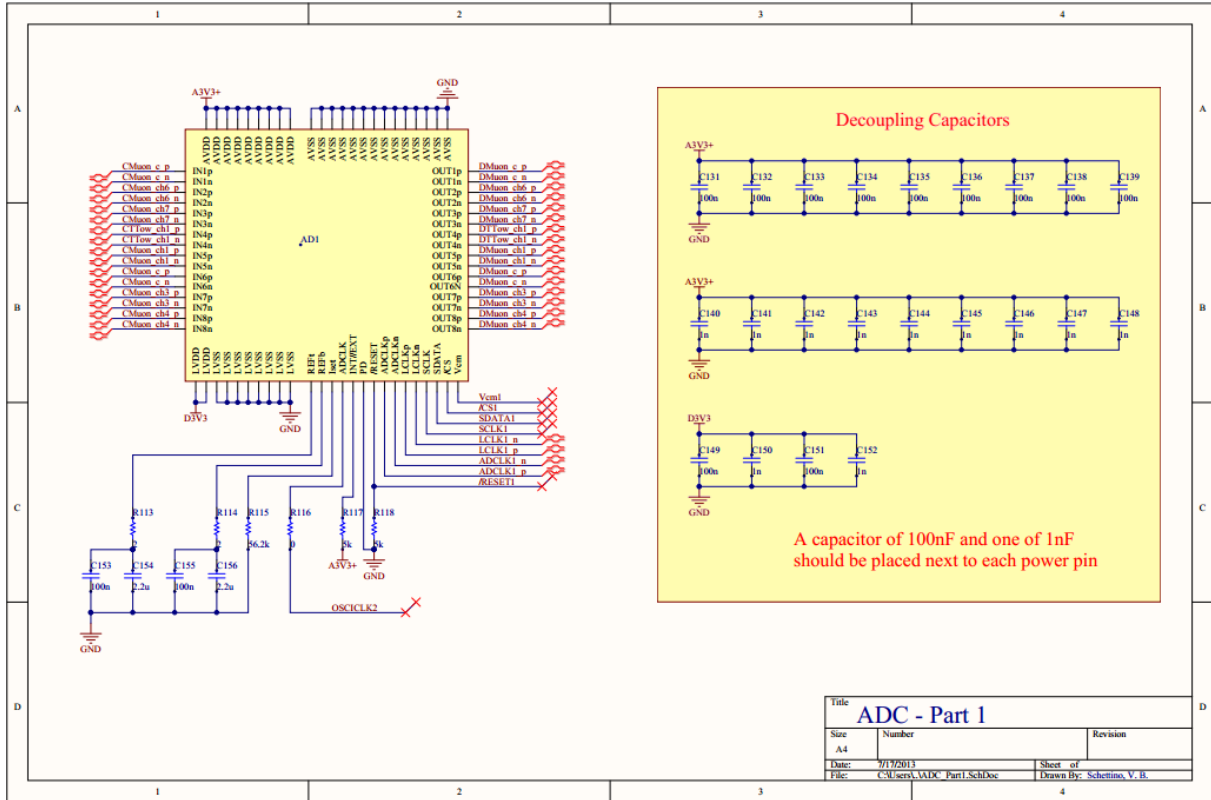Not reviewed, for internal circulation only
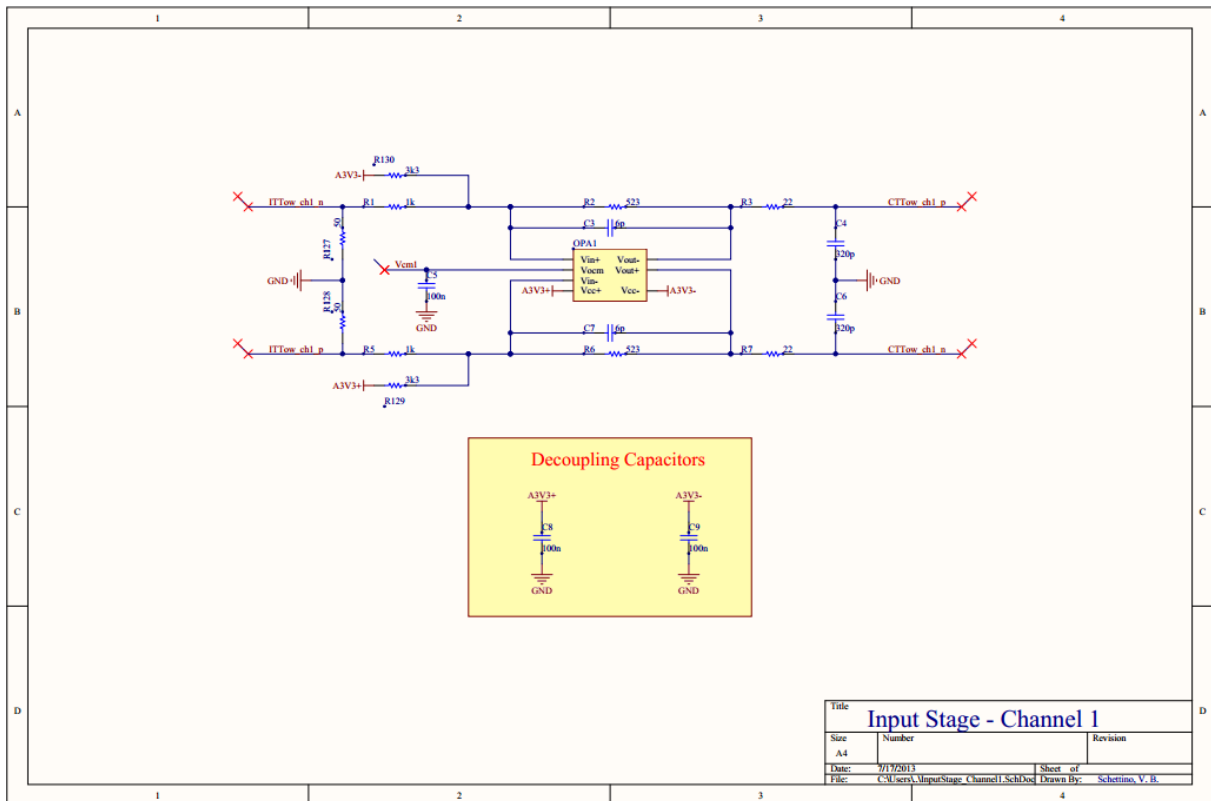

Figure 5: Schematics of the ADC.
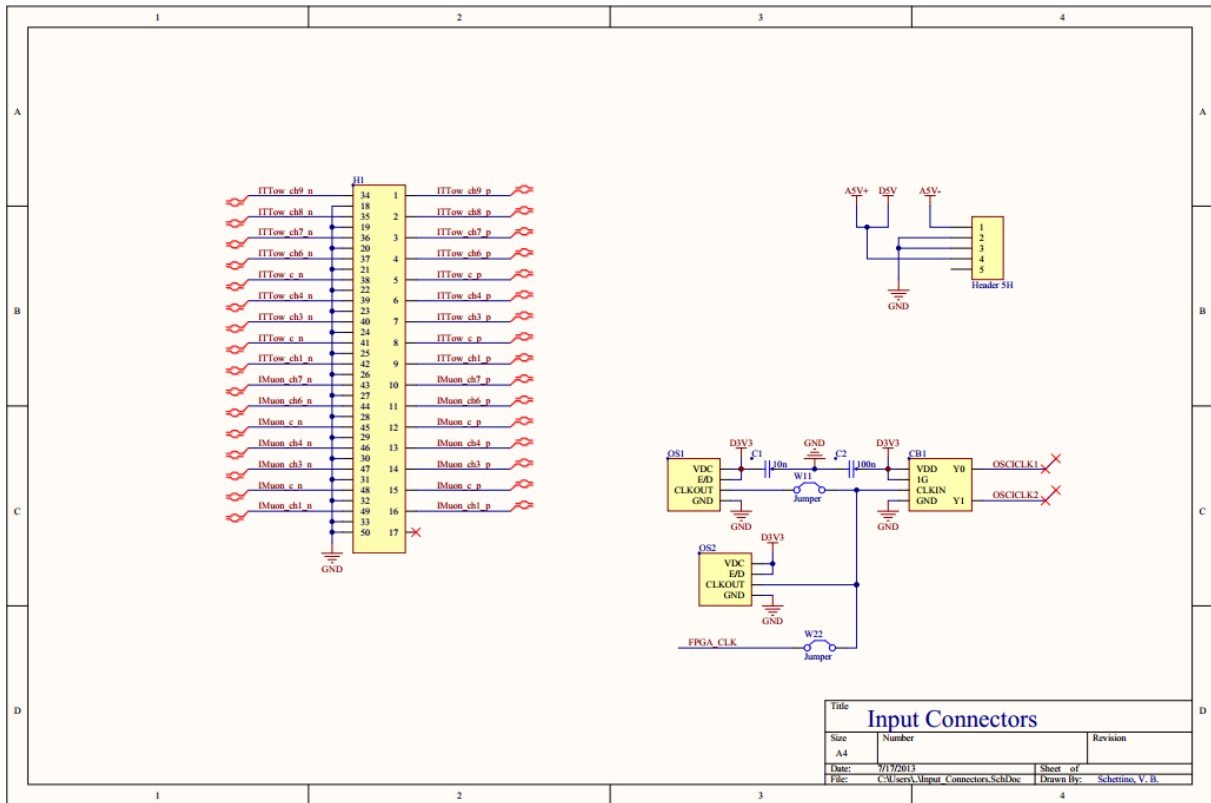
Figure 6: Schematics of the ADC. (Note there is one schematic for each channel totalling 16)

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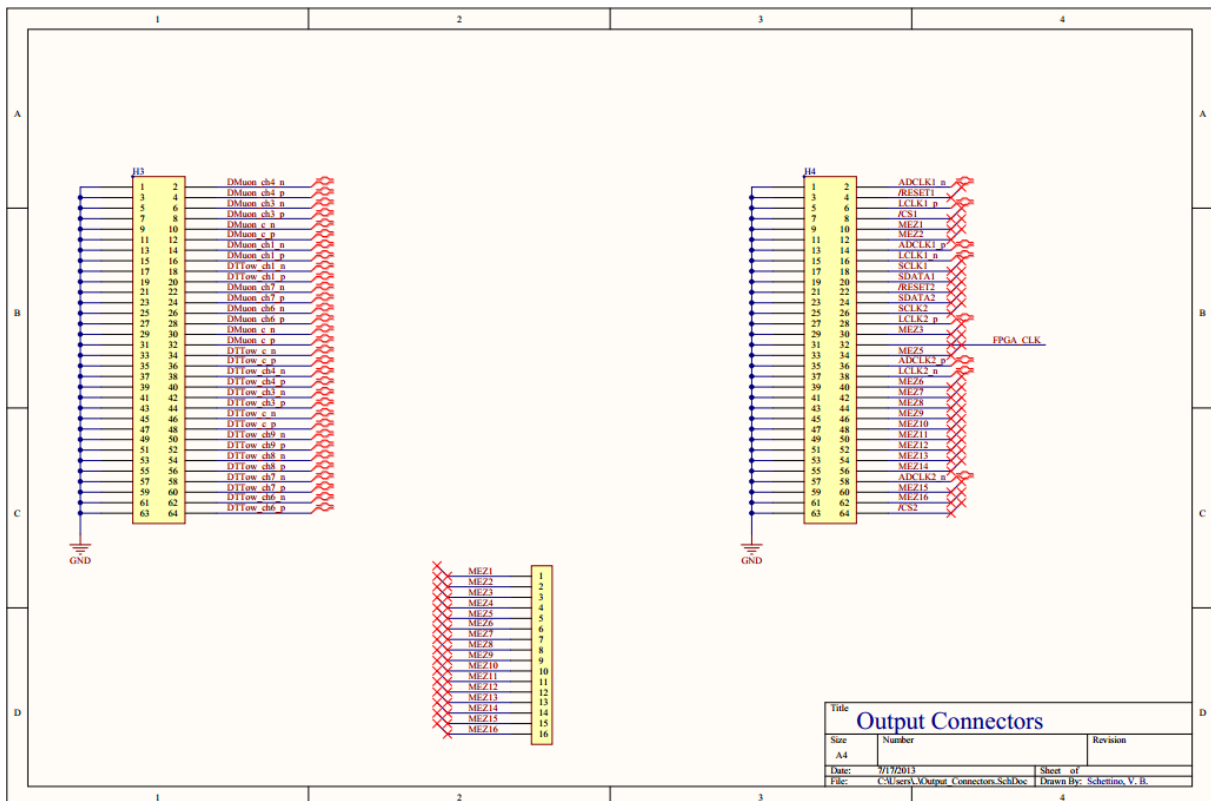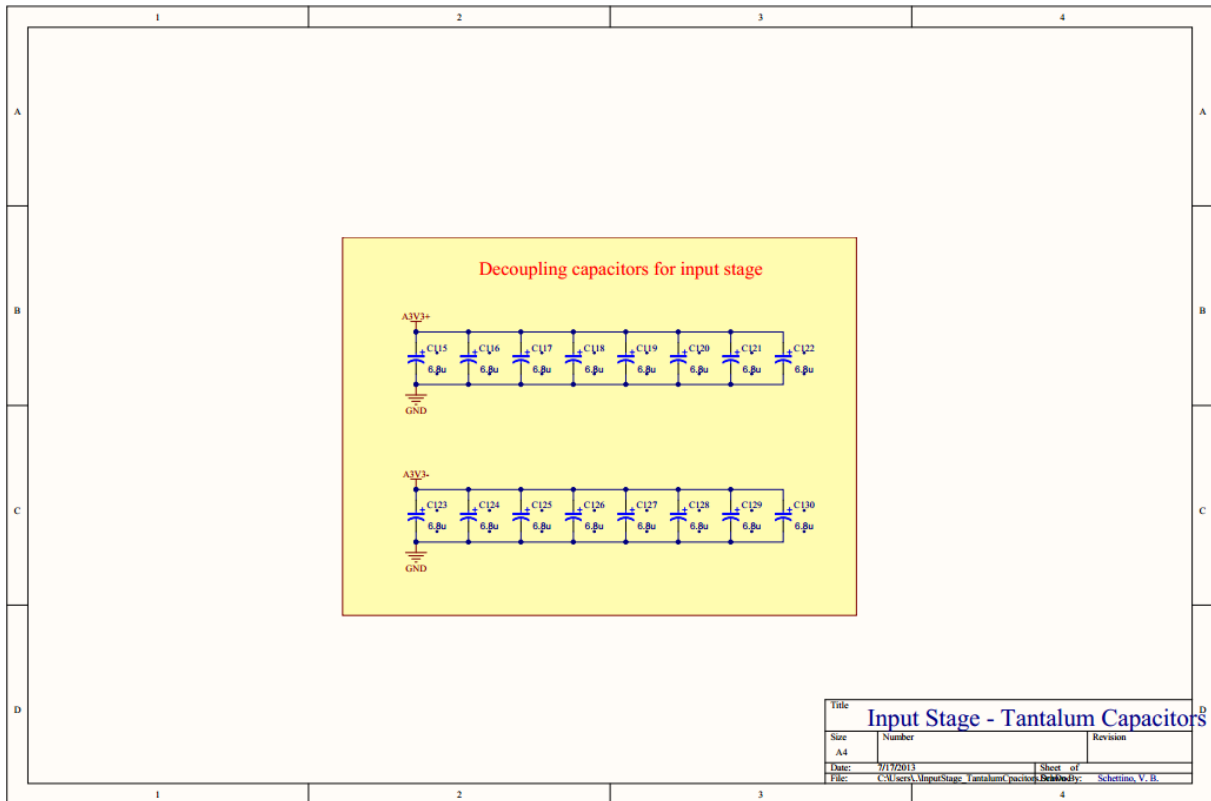
Figure 7: Schematics of the ADC.

2.3   High Voltage Board

The high voltage board has been custom-built for the MobiDICK4 system. This board implements a high voltage power supply that is activated using a TTL controlled relay. It has one input voltage of +24 V with 1 A current which is then converted on the board into an additional +5 V with 100 mA. This is provided by an internal DC/DC IQ2405SA converter. The on/off switch is controlled by a TTL signal (0 V and 3.3 V) and once it is turned on, -830 V is output. The high voltage is provided by an Ultravolt module [6]. This is used to power the gain of the PMTs on the front-end. The HV board is shown in Figure 8.
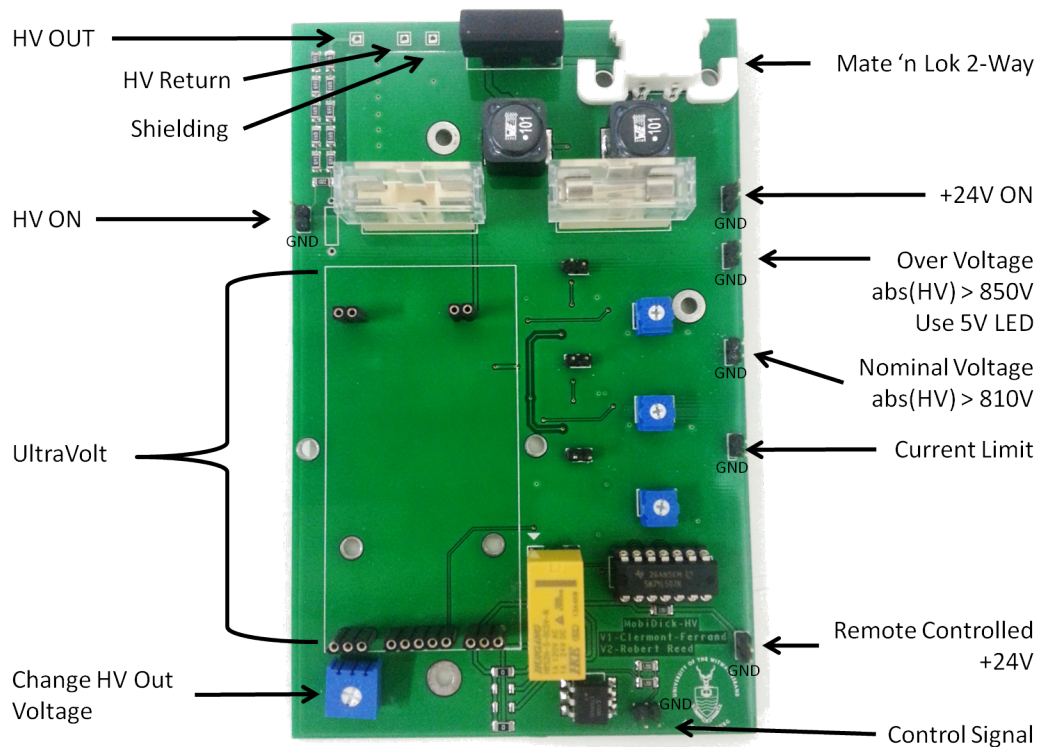
Figure 8: The upgraded High Voltage board

Since we produced multiple versions of MobiDICK4, four HV boards were produced. The board underwent additional modifications in the form of temporary patches that were then incorporated into the final design. A list of all major modifications, that are now permanent features in the board, are given below:

1. A quick fix was introduced to the HV board to isolate it from the motherboard. Isolation is mandatory in the HV board as to avoid any unexpected dark currents. This was achieved by using an optocoupler (This isolates the boards by introducing a one way optical connection). This patch was originally attached onto the HV board and has now been included onto the PCB.

2. To provide the necessary power, a converter was attached onto the +24 V cable to transform it to +5 V DC. This device has also been included on the board which

198 reduces the size and complexity of the power connector and power supply needed.
199 The board requires +24 V to effectively ramp up the Ultravolt module to produce
200 the desired voltage.

201 3. The LED pads have been replaced with pins. This allows the LEDs to be placed
202 further away and connected using standard LED cables to the pins (See Section 2.8).

203 4. The final board design has all the same dimensions and mounting holes (one was
204 moved to make space) so it will be easy to replace the older board. The routing was
205 redone in the final version and some part placements were reconfigured. Components
206 were upgraded when possible such as the old axial inductors with the newer square
207 surface mounted inductors.

208 The schematics of the final design are shown in Fig. 9 and the newly fabricated HV
209 board is shown in Fig 8.

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Figure 9: Schematics of the upgraded High Voltage mezzanine

2.4   LED driver

The LED driver produces two electrical pulses approximate 20 ns wide with a 20 V amplitude and 70 ns time delay. These are created at the rising edge of an input pulse [7] using TTL logic (0 V and 3.3 V). To reduce power consumption and the extended heating of componenets, the onboard 24 V is switched off by default and switched on by the user when needed via another TTL signal. The LED can be powered by either a 24 V source or a 12 V source. Four indication LEDs can be attached to notify users of : on board 5 V on, active input triggering, and the two channels being supplied with V (see Section 2.8). The trigger +3.3 V is provided from motherboard. Figure 2.4 shows the features of the new LED board.
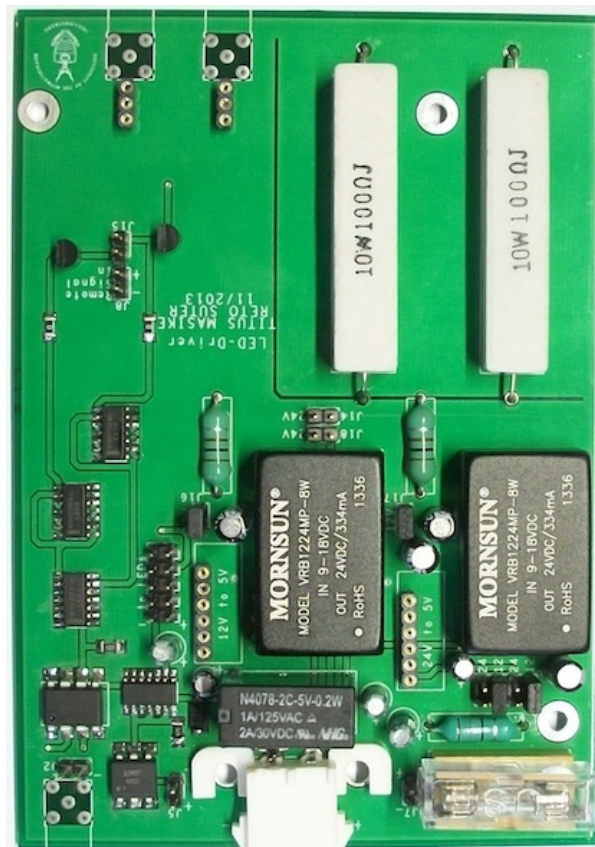
Figure 10: The upgraded LED board

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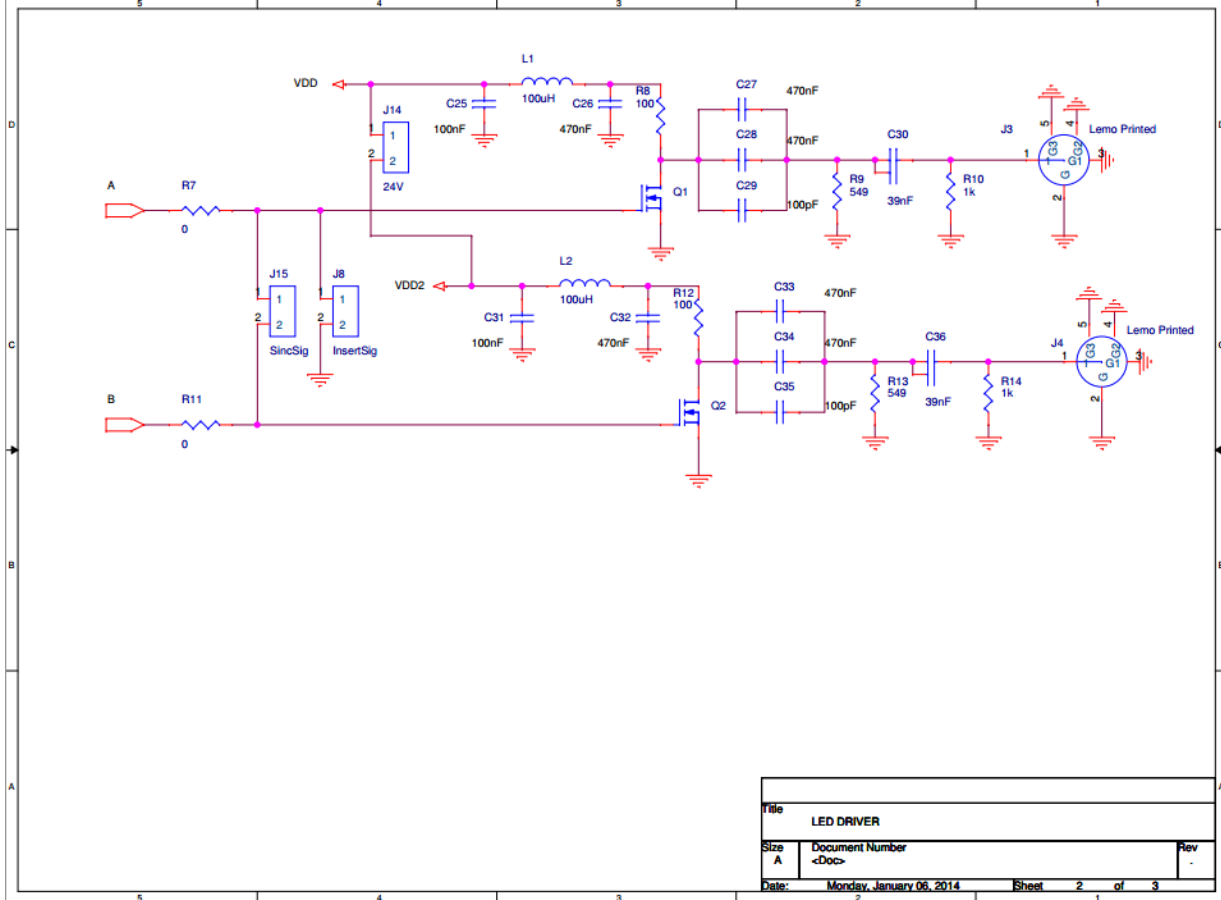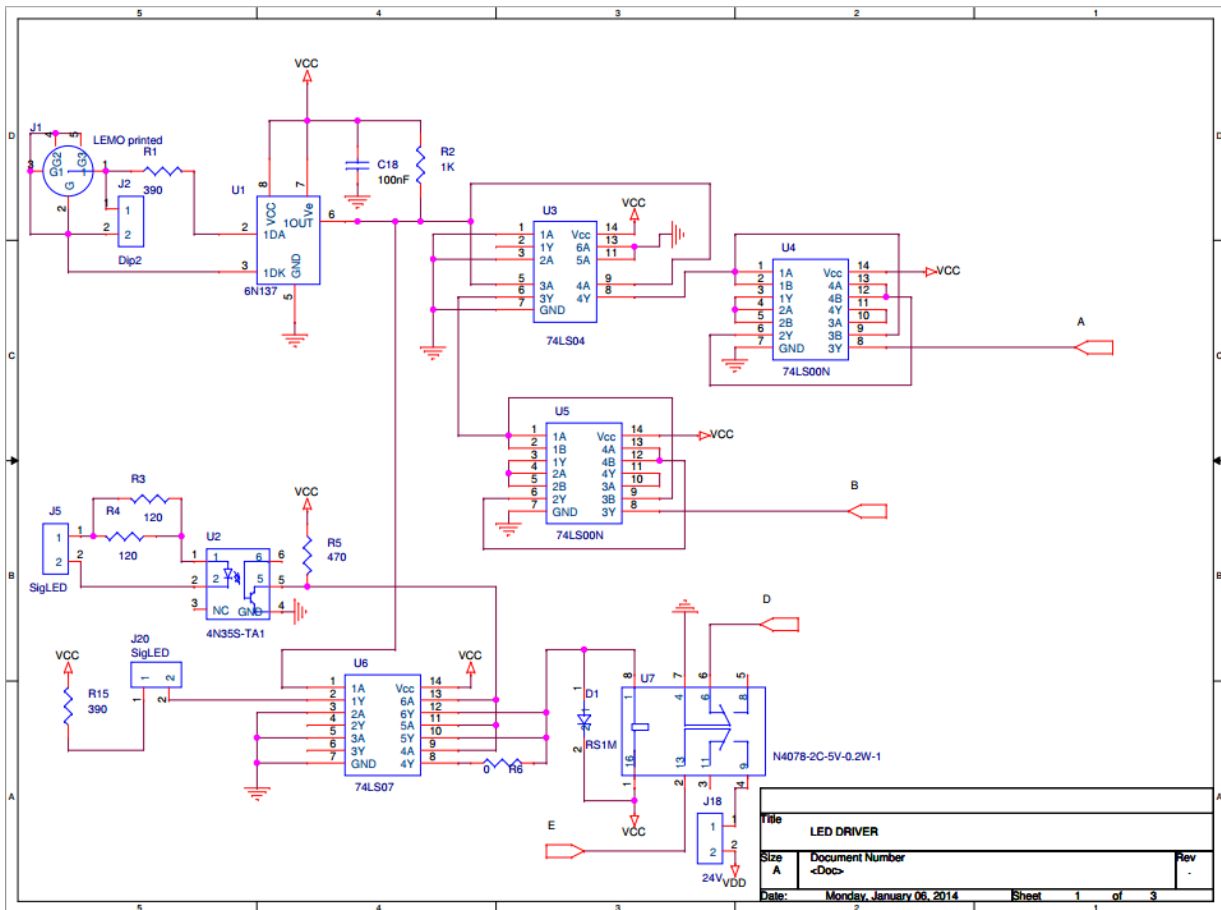
Figure 11: Schematics of the LED Board.
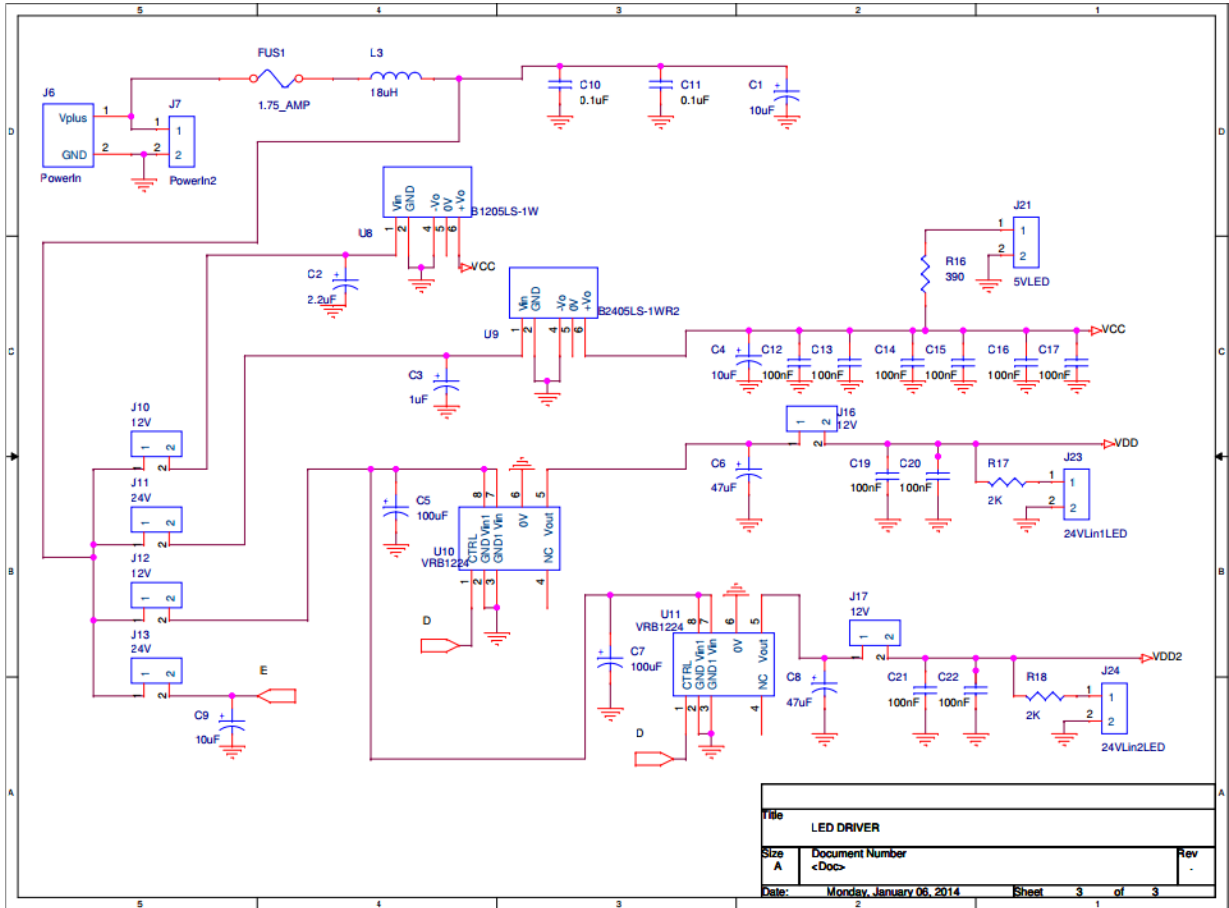
Figure 12: Schematics of the LED Board.

2.5 CAN bus interface

Two LAWICEL CAN232 V3 CAN bus interfaces [8] are available to communicate with the
HV and integrator ADC. The RS232 ports of the motherboard are used to send/receive
commands and are transformed into the CAN protocol using the commercial dongle.
These two CAN bus dongles replace the TVME200 card which holds the TIP816 in the
previous version.

Cabling patch-panel to dongles (SUBD-15 to two SUBD-9). Pins CANL (2) and CANH
(7) must be connected via a 120 Ω resistor. The pin out is detailed in Table 2.
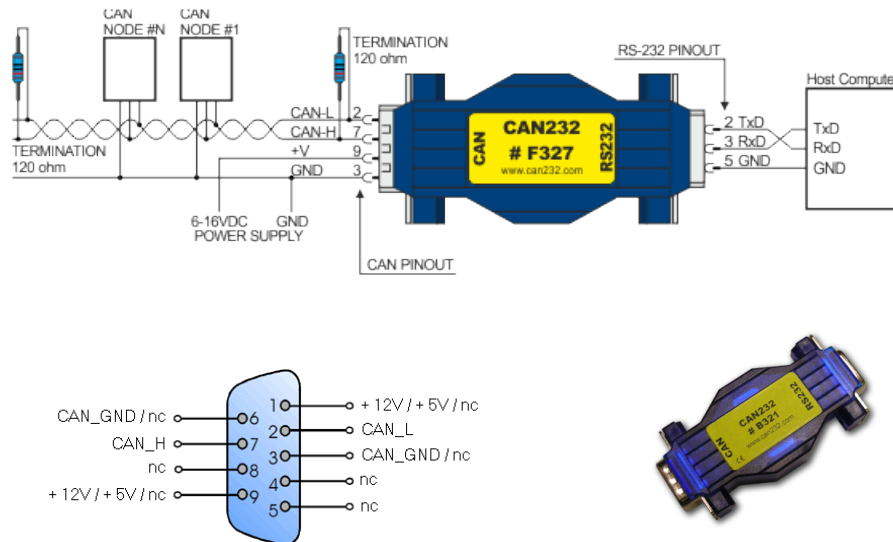
Figure 13: CAN bus connection diagram (top), pin out (bottom left) and the commercial
dongle (bottom right) [8]

The power needed to feed the CAN system is provided by the MobiDICK4 power
supply. Additional power has to be provided at the CAN side of the dongle as specified
from the 12 V of the ATX. The CAN232 dongles are set to a serial baud rate of 115200
baud, the second fastest available. They should not be set to the fastest rate of 230400
baud as they will communicate too fast for the front-end, and are not reprogrammable at
that speed.

Signal	Pin in SUBD-15	Pin in SUBD-9 (ADC)	Pin in SUBD-9 (HV)
Reserved	1		
CAN HV L	2		2
CAN HV G	3		3
Reserved	4		
CAN shield	5	5	5
ADC CAN G	6	3	
ADC CAN L	7	2	
Reserved	8		
Reserved	9		
HV CAN H	10		7
Reserved	11		
HV CAN V+	12		9
Reserved	13		
ADC CAN V+	14	9	
ADC CAN H	15	7	

Table 2: CAN bus pin out interfacing [8]. Note V+ and G are +12 V and 0 V respectively.

2.6 Networking

A commercial networking router is used to provide a static DHCP address to the motherboard on the LAN side and a public IP address on the WAN side. The firmware running on the motherboard forces the the MAC address of device to be CA:CA:CA:CA:CA:CA which is then permanently assigned in the router to the address 192.168.0.102. In this way, the firmware in all motherboards is the same, and so is the IP address of the motherboard in the LAN. Furthermore, the router is configured with the IP address 192.168.0.1 in the LAN.

The model of the router used in MobiDICK4 is a DLink Dir-100/E that has four LAN ports and one WAN port as shown in Figure 15 and uses 5V as input voltage. One LAN and the WAN port are made available through the front-panel, so that the user can chose to connect directly to the LAN port where MobiDICK will be available in the static IP address mentioned before, or connect through the public network when the box is connected through the WAN port to an external network. In this case the following ports have to be forwarded from the static IP address to the public address in the router's configuration: port 21 for FTP access, port 23 for telnet access, and port 1570 for MobiDICK accesss.

Figure 14: DLink router Dir-100/E [9] placed inside the MobiDICK box.

2.7 Power Supply

MobiDICK4 has two separate power sources. One is a commercial ATX power supply and covers most of sub components and daughter boards. The second is an LS150-24 AC/DC that provides 24 V. In Table 3 the voltage requirements by different boards are listed. Tables 4,5,6,7 and 8 show the pinouts for the connectors and the cabling color for the main components.

Voltage	Source	Color	ML507	Router	ADC board	LS 150	HV driver	LED driver
+5 V	ATX	Red	yes	yes	yes			
-12 V	ATX	Blue			yes			
+12 V	ATX	Yellow						
GND	ATX	Black	yes	yes	yes	yes (-V)		
220 VAC	ATX	-				yes		
+V	LS150	Purple					yes (+24 V)	yes (+24 V)
-V	LS150	Brown					yes (0 V)	yes (0 V)

Table 3: Voltage requirements by the different boards

Voltage	Color	LS150 Pin
220 VAC+	Grey	L
220 VAC-	Blue	N
0 V	Black	V-

Table 4: Cables for LS150: Connectors LUGS EDH 04.76.22.224.1e

Voltage	Color	ML507 Pin
0 V	Black	1
+5 V	Red	2

Table 5: Connector for ML507 and Router : Pole

Voltage	Color	ADC Pin
-12 V	Blue	1
0 V	Black	2
0 V	Black	3
+5 V	Red	4

Table 6: Connector for ADC board: AMP Mate-n-lock 1-480424-0 with female pins

Voltage	Color	LED Pin
+24 V	Red	1
0 V	Black	2

Table 7: Connector for LED board: Mate-n-lock 2 way with male pins

Voltage	Color	HV Pin
+24 V	Red	1
0 V	Black	2

Table 8: Connector for HV board: Mate-n-lock 2 way with male pins

2.8   Indicator Interface

Information on the status of MobiDICK is presented through a commerical backlight LCD screen and several LED lights. The LCD Screen allows the user to see small text messages from the system as the tests are performed in order to monitor the correct performance of the box. The model used is a MIDAS MC21605J6W-FPTLW that connects with a dedicated pin-out to the motherboard and to a +12V and ground. A 10k Ohm resistor is used in series to step down the +12V to an appropriate value for the LED backlight. This device is very delicate, for which a dedicated cabling is made in such a way that there is no possibility of connecting the display in the opposite direction.

Pin on LCD	Pin on Motherboard	Power
1	2	-
2	1	-
3 to 14	3 to 14	-
15	-	+12V
16	-	Ground

Table 9: Cabling for the LCD.
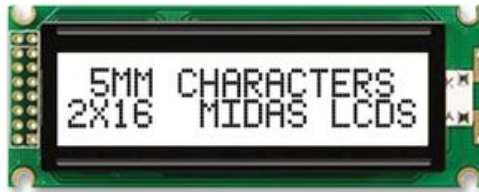
Figure 15: LCD used in the front-panel of MobiDICK.

The indicator LEDs are put at the left top corner of the front panel and indicate the status of the CANBus power and LED/HV board (Fig. 16). The are, from left to right:

1. CAN Fuse: A green LED to show the status of the CANbus fuse. If it is off, the fuse should be replaced. The CAN Fuse LED requires a 1k Ohms resistor in series with the CANbus power.

2. HV +24V: A green LED to show that the HV board is on and receiving +24V.

3. HV On: A white LED to show that the HV supplied to the super drawer has been turned on.

4. HV Over Voltage: A red LED that states the HV is outputting a larger than expected voltage. After extended use, the HV may drift to a higher voltage value (roughly 900V) that is not safe for the pmts. The HV Over Voltage LED requires a combination of a 15 k Ohms resistor in series with the LED, and then a 10k Ohms resistor in parallel with the combination.

5. LED On: A white LED shows that the LED board is actively being pulsed. It will be on for the duration of the LEDon test.

Label	Color	MobiDICK4 cabling
CAN Fuse	Green	CANbus power after fuse + ground
HV Fuse	Green	HV board J1 (+24V on)
HV ON	HLMP-CB50 blue	HV board J6 (HV output)
OVC	Red	HV board J2 (Over voltage)
LED ON	HLMP-CB50 blue	LED board J2 (Trigger input)

Figure 16: The indicating LED on the front end of MobiDICK4

2.9 Casing and cabling

The SFP transceiver module is being used for the communication with the super-drawers and has to be purchased separately. The current version we are using for MobiDICK4 is an SX type working at a wavelength of 850 nm and operates at 3.3 V. There are two cable latches: one for the receiver section (RX) and the other for the transmitter (TX). Two coaxial optical cables are connected with a 6.25 mm separation gap. The data from the PMTs in the super-drawer is transmitted through TX while Trigger Timing and Control (TTC) commands are received through the RX. The SFP module is shown in Figure 17.

Figure 17: The SFP SX type module

The physical layout of MobiDICK4 is one of the most distinctive features with respect to the former model. A comparatively smaller size (length of 350 mm, width of 450 mm and height of 200 mm) and lighter weight (4 kg) add mobility to the new system.

The CAN bus fuse is located at the top right corner of the front panel and can be replaced easily. Two LED Lemo outputs are placed just under the fuse. The HV board is needed when one uses the LED board. Therefore, the blue LED on the top left corner will be on.

All the connection cables except the power cable are mounted the at the front panel as well. Two trigger connections, one for muon trigger and the other one for tower trigger, are under the LED arrays and the HV source is provided from the connection located next to the tower trigger cable. There are two Ethernet ports on the front panel (bottom middle and bottom right) that communicate to the WAN link of the router to provide
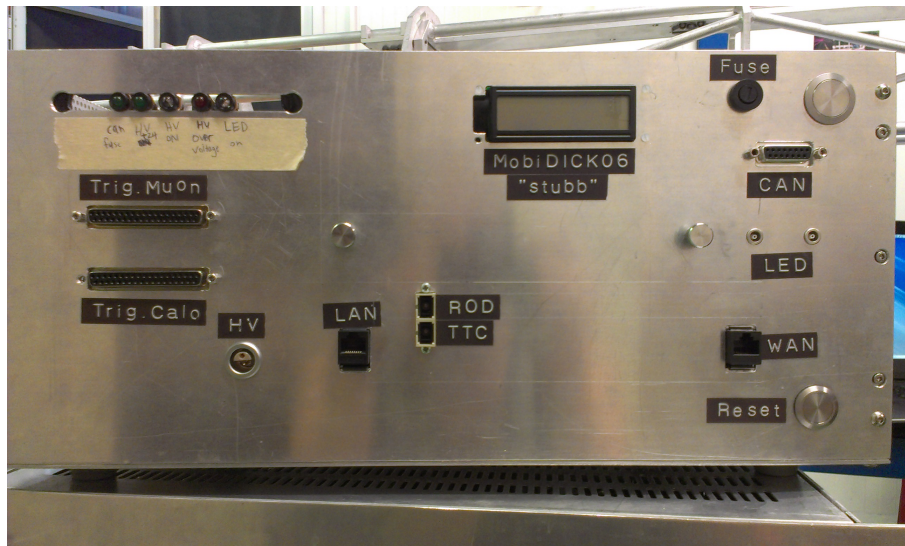
Figure 18: MobiDICK4 exterior feature

external network access to the system. ROD and TTC fiber optic cables are connected in the central area of the front panel. There is a reset button at the bottom right corner to reboot the motherboard if the system trips. A second reset button at the top right corner will reset power to the CAN232 dongles in case CANbus communication is interrupted (e.g. by aborting a test). There is a handle to carry the new MobiDICK on the right-hand side of the system and the system can sit vertically on four pads on the left-hand side of the box. Each side of the box has been finished with mesh pattern for the air flow. On the back panel the power cable is connected next to the system power switch.

2.10   Laptop

A linux laptop is needed to run the front-end GUI software, called Willy. SLC6 is the prefered linux distribution and is well supported by CERN. It is possible to run Willy on SLC5 or Ubuntu, but it is not recommended. Four laptops have been purchased, and their numbering is from 4 to 7 to correspond with the MobiDICK units (though any laptop may be used with any MobiDICK). Laptops #4, #5, #6, and #7 are a HP ProBook 4545s, a HP ProBook 4520s, and two DELL Latitude E6540, respectively. A laptop communicates with MobiDICK4 through a direct Ethernet connection, and proper communication requires the wifi of the laptop to be turned off. This can be done through the network settings on laptops #4 and #5, or through a switch on the right hand side of laptops #6 and #7. While tests are running with Willy, the local or central database that matches with the associated super-drawer would be accessible from the laptop. Requirements for the laptop are:

- Ethernet connection port

- Linux OS (slc6 preferable)

- Software packages: xterm, telnet and spawn.

326   • CERN ROOT

327   • Willy software installed (see section 5)

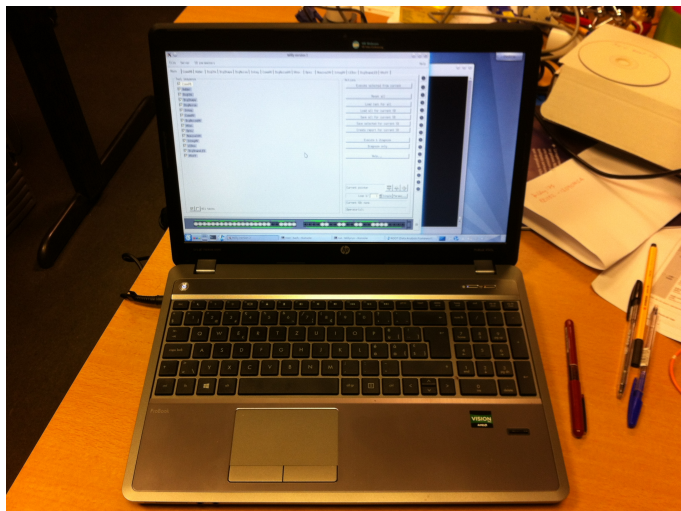

Figure 19: Laptop for the MobiDICK4

3   Hardware Tests

3.1   ADC

3.1.1   Pulse shape

The analog output of the super-drawer can be monitored with the system acting as a digital scope. The samples output by the board are inverted, where 4095 corresponds to zero. Up to 128 samples can be stored at a time in the FPGA. Figure 20 shows an example of one sampling for the pulse shape measurement at different charge injection times.
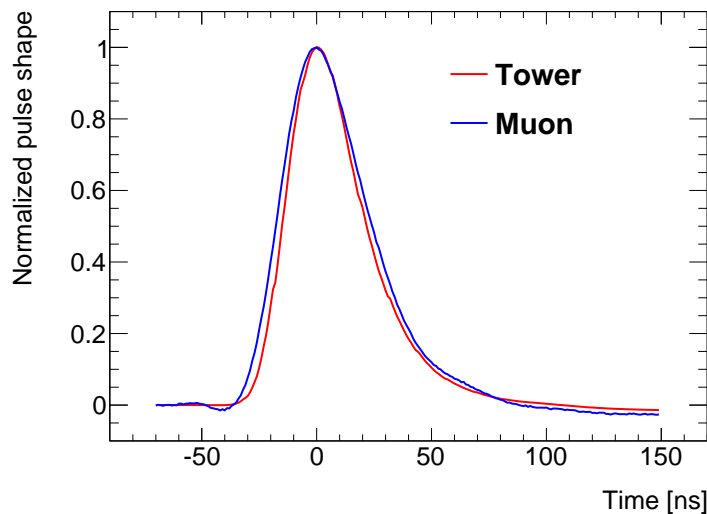

Figure 20: ADC pulse shape measurement example with a time variation of the charge injection

Figure 20 and the pulse shape measurement of the tower and muon output of the super-drawer were performed by MobiDICK by sampling a known charge at different time offsets as shown in the bottom picture of Figure 20. As expected, muon output has a slightly wider distribution, compatible with previous measurements.

3.1.2   Linearity tests

In Figure 21 and Figure 22, all the channels of the ADC board have been tested and reconstructed by two different methods: the Flat Filter and the Optimal Filter [10]. As we see in the figure, the linearity of the reconstructed energy as a function of different charges is very good for both Flat and Optimal Filters. The difference between these two methods is not significant.

The responses of the ADC channel for a given charge are uniform overall. The uniformity of the ADC channels is shown in Figure 22. The top plot in each channel's test is the reconstructed response versus channels and the bottom is the deviation from the mean. Both Flat Filter and Optimal Filter responses agree as seen in the same figure. Differences between the ADCs can be further improved by inter-calibration if needed.
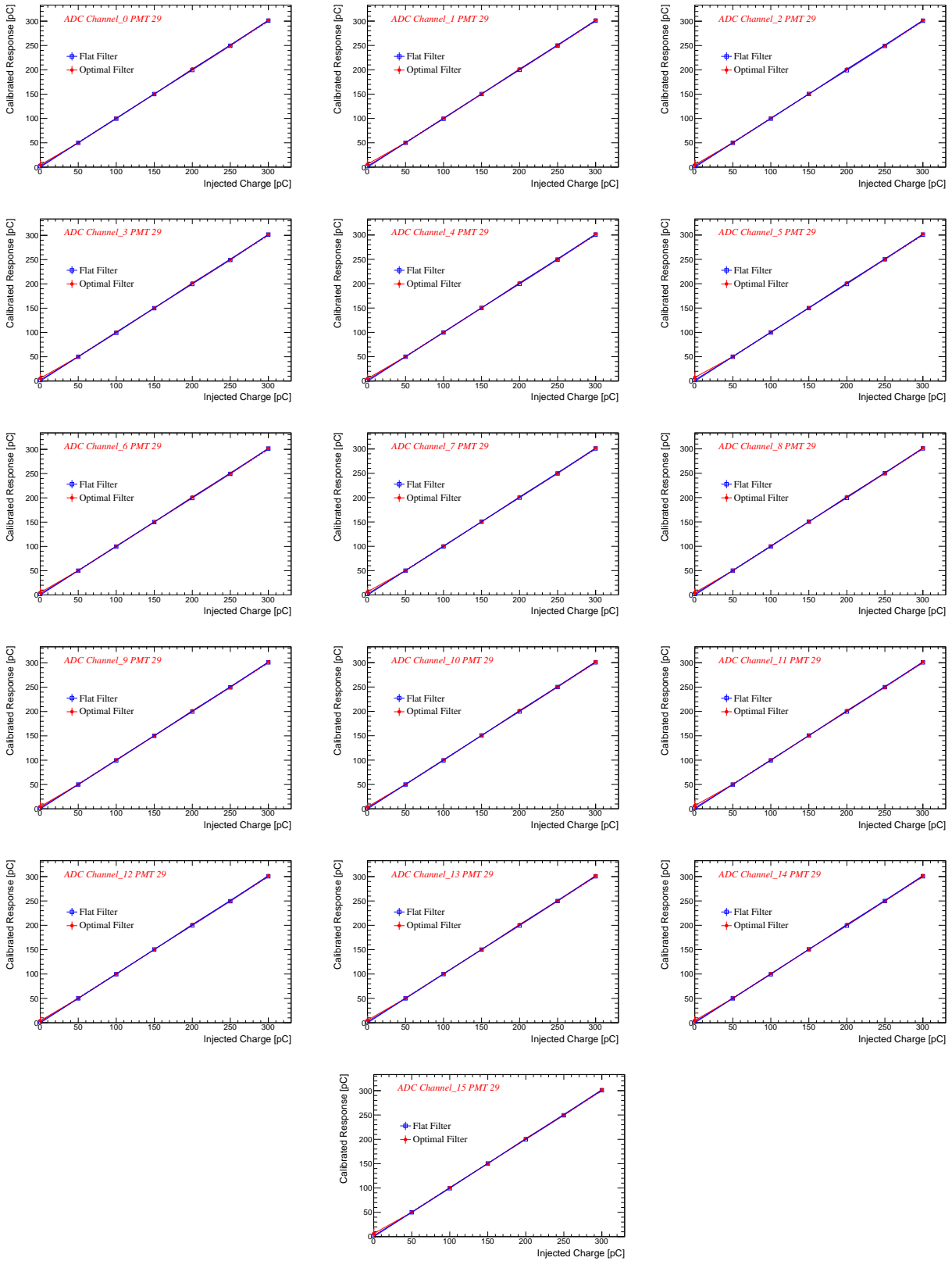
Figure 21: Calibrated responses of all ADC channels as a function of injected charge.
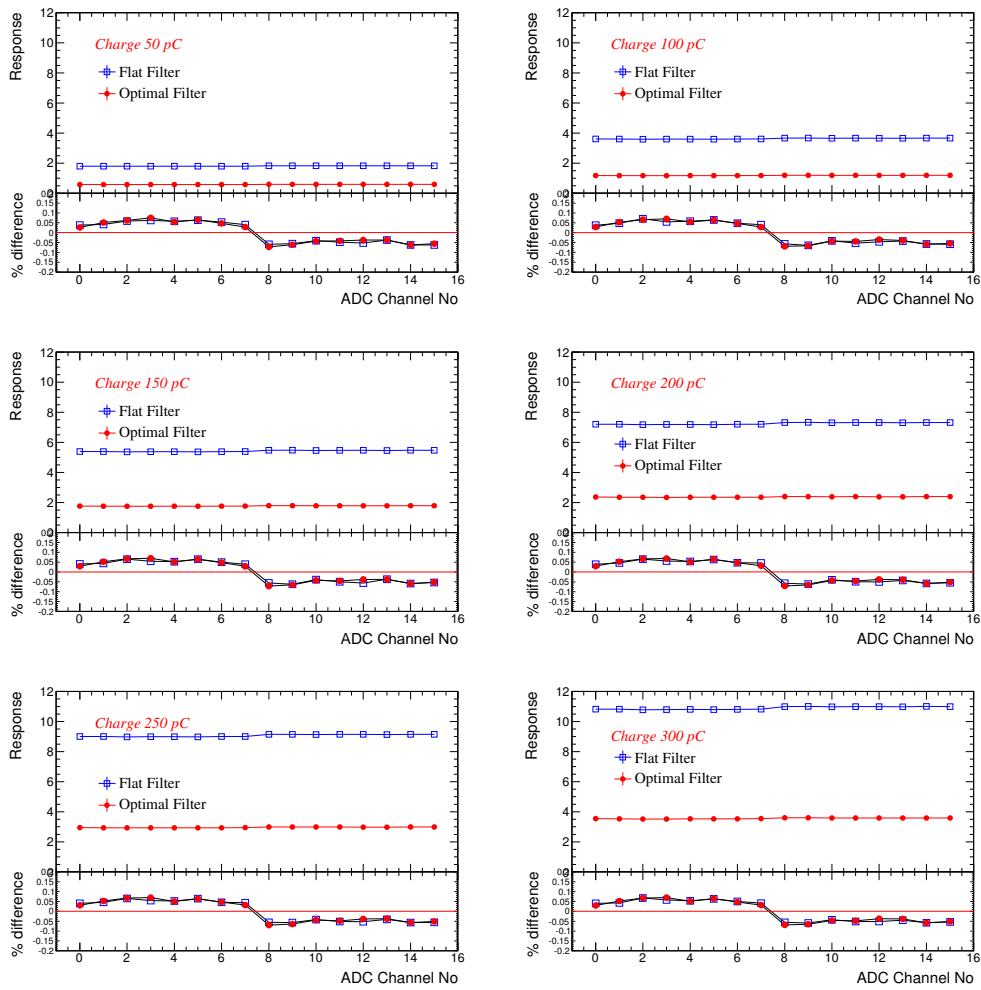
Figure 22: Uniformity of the channels in the ADC board reconstructed at the given charge which is varied from 50 to 300 pC.

3.2   High Voltage Board

3.2.1   Propagation Time

It is useful to determine how long it takes for the high voltage to turn on once the input signal has been sent. If this takes too long then tests pertaining to the Photo Multiplier Tubes, which are powered by the HV board, must be delayed before commencing. An oscilloscope was connected to the HV board so that Channel 1 (Blue) was connected to the Input Signal and Channel 2 (Red) was connected to the HV Out at the HV LED so as not to burn out the scope with -800V. Refer to Fig. 23. The time taken between the activate request and HV output is approximately 9.1 *ms*. This is fairly slow but is attributed largely to the mechanical relay switch.
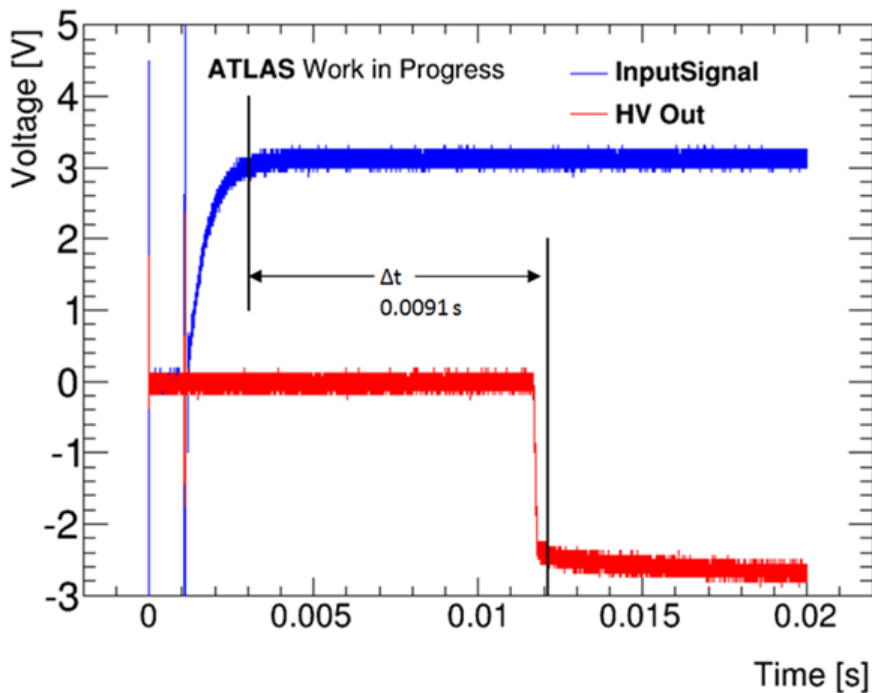
Figure 23: Input and output channels during HV activation.

3.3   LED Board

3.3.1   Propagation Time

It is useful to determine how long it takes for the LED to pulse after the input signal is received for reasons similar to the High Voltage Board. The method to determine the propagation time is identical. Channel 1 was connected to the input signal and Channel 2 was connected to the signal output of the board. Measuring the delay between the rise of each gave the time propagation to be 70 *ns* ± 15 *ns*.

4   Firmware

The firmware is developed with Xilinx ISE and EDK version 13.1. Table 10 summarizes the base addresses of each component.

Device	Base address
HV+LED	0xC8600000
ADC1	0xD8600000
ADC2	0xD9600000
TTC	0xE8600000
SysMon	0xE8610000
Orbit	0xE8620000
Glink	0xF8600000
LCD	0xF9000000

Table 10: Base registers of the embedded system

The firmware and linux image are copied into the Compact Flash (CF) which is then plugged into the mainboard. During the power up sequence the firmware and linux image are loaded into the FPGA and CPU from the CF respectively.

4.1   Embedded system

Each component has a dummy register at address zero (0x0) for testing the access to the component. Figure 24 shows a representation of the embedded system. The PLB bus is used to communicate with the different IP cores. The core of the embedded system is an IBM PowerPC 440 running at 400 MHz which communicates with different IP cores using the Processor Local Bus (PLB). The embedded system controls all the external devices using the integrated components on the board such as two serial ports, DDR2 memory controller, flash memory controller, Ethernet chip, hard Ethernet, system monitor, HV and LED driver controllers, ADC trigger controller, TTCvi emulator, and G-Link decoder. This embedded system replaces the TTCvi, TTCex and ODIN cards. VHDL code is available to control the different devices of the board, including TTCvi and G-Link emulators which are interfaced by software from the previous versions.

4.2   G-Link

The G-Link core is the interface with the read-out of the digital data. It has two operation modes: normal and CRC.

- In normal mode, it stores the event frame words on a FIFO of 2048 32-bit words. The event frame is initialized by the start of event word 0x51115111. To reset the FIFO, bit number 0 of the control register has to be set to 1.

- In CRC mode, each event fragment is checked for digital errors and CRC mismatch. The results are stored on the appropriate registers. To reset the error registers, bit number 1 of the control register has to be set to 1.
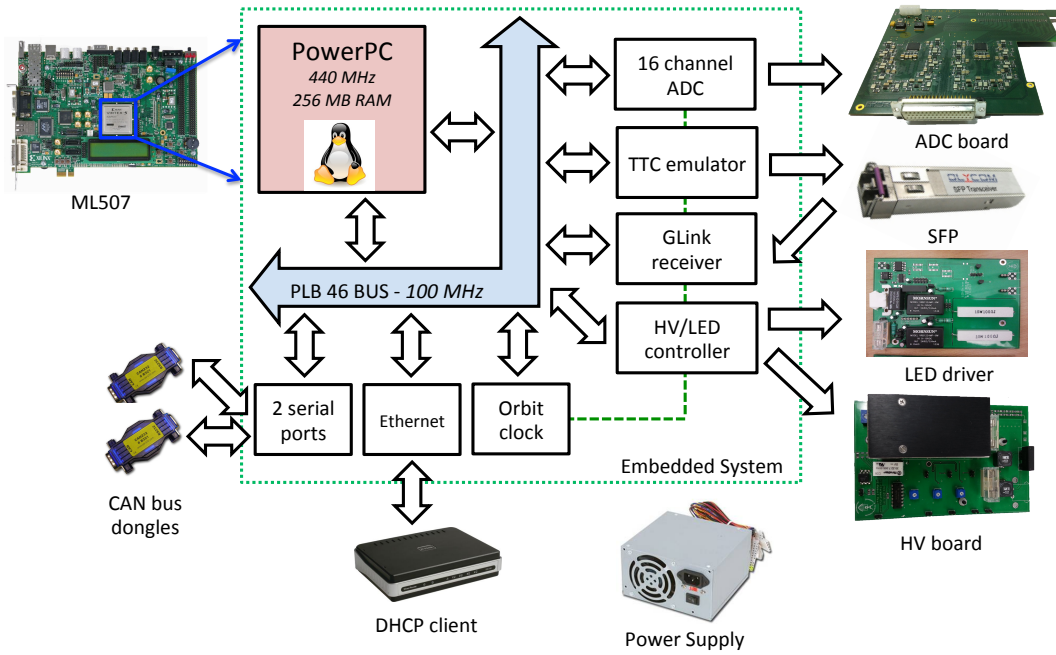
Figure 24: Embedded system

The CRC mode has two operation modes: extended mode or normal mode, depending on the source of the data, either from an extended barrel module or a long barrel module. In order to set the operation modes, bit 3 or bit 2 have to be set to 1 to select the mode. Table 11 shows the possible values of the control register.

Register	Offset	Access	Description
Dummy	0x0	W/R	Dummy register to test read and write functionality
Status	0x4	R	Bit 31 = GTX is aligned, bit 30 = GTX is re-aligned, bit 29 = GTX detects comma words, Bits 23 - 0 = Release date
FIFO Status	0x8	R	Number of 32-bit words available to read. Diff pos write and pos read
Control	0xC	W/R	0 = Normal mode, 1 = Reset RAM pointers, 2 = Reset CRC counters, 3 = Enable CRC mode. The possible values of the control register are: 0 0 0 0 - Normal Mode (NM) 0 0 0 1 - Reset the FIFO pointers in NM 0 1 0 0 - CRC mode for long barrel (LB) 0 1 1 0 - Reset error counters + stay in LB 1 0 0 0 - CRC mode for extended barrel (EB) 1 0 1 0 - Reset error counters + stay in EB
Data	0x10	R	Read one 32-bit word from pos read and increment the pointer if pos read < pos write
Error Global	0x14	R	Total Global CRC error count
Error DMU Even	0x18	R	Total DMU CRC error count (Even data bits)
Error DMU Odd	0x1C	R	Total DMU CRC error count (Odd data bits)
Checked Events	0x20	R	Number of checked events
Error DMU mask	0x24	R	16 bits indicating the DMU with error
ERROR BIT 31 or 17 DMU 1 & 2	0x28	R	
...			
ERROR BIT 31 or 17 DMU 15 & 16	0x44	R	
ERROR PARITY DMU 1 & 2	0x48	R	
...			
ERROR PARITY DMU 15 & 16	0x64	R	
ERROR MEMORY DMU 1 & 2	0x68	R	
...			
ERROR MEMORY DMU 15 & 16	0x84	R	
ERROR SSTROBE DMU 1 & 2	0x88	R	
...			
ERROR SSTROBE DMU 15 & 16	0xA4	R	
ERROR DSTROBE DMU 1 & 2	0xA8	R	
...			
ERROR DSTROBE DMU 15 & 16	0xC4	R	

Table 11: G-Link registers

4.3 TTC

₃₉₉

₄₀₀ Trigger Timing and Control (TTC) is a multi-purpose distribution system for front end
₄₀₁ synchronisation based on fiber optics.

₄₀₂   Accepted triggers, trigger information, event count various calibration, control, reset
₄₀₃ and test commands can be sent over the TTC network. Table 12 summarizes the registers
₄₀₄ needed by the TTC IP core to send commands over the TTC network or TileCal. This
₄₀₅ core is not specific to MobiDICK and can be reused for other development.

Register	Offset	Access	Description
Dummy	0x0	W/R	Dummy register to test read and write functionality
Status	0x4	R	Bits 23 - 0 = Release date
A channel	0x8	W/R	Register to manipulate A commands: Single and multiple L1As, fixed rate triggers
B channel Asyn	0xC	W/R	Register to write asynchronous B channel commands
B channel Syn Control	0x10	W/R	Control of the FIFO of synchronous commands. Bit 31 = 1 execute stored commands on each orbit. Bit 30 = 1 reset the FIFO.
B channel Syn FIFO	0x14	W/R	Command (bits 31-23) and offset wrt orbit in units of BC (bits 15-0) to store in the FIFO. Special commands (longer than a short command) start at bit 16: L1A = 0x7FFF, LED trigger = 0x0FFF.

Table 12: TTC registers

4.4 Orbit

₄₀₆

₄₀₇ The orbit signal is a square wave of period 88.924 μs which corresponds to 3564 bunches
₄₀₈ with a frequency of 40.08 MHz [11]. These orbit signals can be accessed through the
₄₀₉ registers listed in Table 13.

Register	Offset	Access	Description
Dummy	0x0	W/R	Dummy register to test read and write functionality
Status	0x4	R	Internal status of the IP core
Control	0x8	W/R	0=Off; 1=Generate the Orbit clock; 2=Single pulse

Table 13: Orbit registers

₄₁₀   This module allows the generation of a local orbit clock which is used to gate the
₄₁₁ generation of signals stored in the TTC B channel synchronous memory.

4.5   ADC

The ADC firmware implements a memory to store 100 samples from all the channels of the ADCs. The memory is filled upon the execution of the 0x1FFF special command in the TTC IP core. 16 pointers reference the writing position for each channel. The remaining 16 independent pointers mark the reading position inside the memory. Each time a write request is executed, the read pointers are reset to zero. Table 14 lists the registers of the ADC board.

ADC no.	Base	Register	Offset	Access	Description
ADC1	0xD8600000	Dummy	0x0	W/R	Dummy register to test read and write functionality
		Status	0x4	R	Bits 23 - 0 = Release date
		Control	0x8	W/R	0x000=Normal mode, 0x100=Reset ADC, 0x200=General Reset, 0x300=Reset pointer, 0x400=Re-align clock
		Data1	0xC	R	Read sample from channel 1
		Data2	0x10	R	Read sample from channel 2
		Data3		R	Read sample from channel 3
		Data4		R	Read sample from channel 4
		Data5		R	Read sample from channel 5
		Data6		R	Read sample from channel 6
		Data7		R	Read sample from channel 7
		Data8	0x28	R	Read sample from channel 8
ADC2	0xD9600000	Dummy	0x0	W/R	Dummy register to test read and write functionality
		Status	0x4	R	Bits 23 - 0 = Release date
		Control	0x8	W/R	0x000=Normal mode, 0x100=Reset ADC, 0x200=General Reset, 0x300=Reset pointer, 0x400=Re-align clock
		Data1	0xC	R	Read sample from channel 9
		Data2	0x10	R	Read sample from channel 10
		Data3		R	Read sample from channel 11
		Data4		R	Read sample from channel 12
		Data5		R	Read sample from channel 13
		Data6		R	Read sample from channel 14
		Data7		R	Read sample from channel 15
		Data8	0x28	R	Read sample from channel 16

Table 14: ADC registers

4.6 HV and LED

The HV and LED IP cores control the HV and LED boards through the series of registers in Table 15. The HV can be turned on and off while the LED can be asserted (constantly on), single triggered, or triggered by the special command (0x...) from the TTC firmware module.

Register	Offset	Access	Description
Dummy	0x0	R/W	Dummy register to test read and write functionality
Status	0x4	R	Internal status of the IP Core FSM
HV control	0x8	W/R	0=Off, 1=On. Turn on/off the HV control through constant voltage on pin J6-12
LED pulse	0xC	W	0=Off, 1=On, 2=Wait for a LED FIFO command, 3=Pulse. Generate a 20 ns width pulse on J6-10

Table 15: HV and LED registers

4.7 System monitor

MobiDICK4 is able to monitor the temperature of the system and activate an alarm in the event of overheating. The registers of the system monitoring (listed in Table 16) are read only.

Register	Offset	Access	Description
ALMout	0x8	R	Temperature alarm output status
Temp	0xC8	R	Present temperature value

Table 16: System Monitor registers

4.8 LCD

MobiDICK4 has an LCD which has been designed to display a brief message about the status of an operation. The registers in Table 17 are used to access specific characters in the display.

Register	Offset	Access	Description
Dummy	0x0	W/R	Dummy register to test read and write functionality
Status	0x4	R	Bits 23 - 0 = Release date
Reg0	0x8	W/R	first row, characters 1 to 4
Reg1	0xC	W/R	first row, characters 5 to 8
Reg2	0x10	W/R	first row, characters 9 to 12
Reg3	0x14	W/R	first row, characters 13 to 16
Reg4	0x18	W/R	second row, characters 1 to 4
Reg5	0x1C	W/R	second row, characters 5 to 8
Reg6	0x20	W/R	second row, characters 9 to 12
Reg7	0x24	W/R	second row, characters 13 to 16

Table 17: LCD registers

5   Software

The software in MobiDICK4 is split into a server (MobiDICK) and client (Willy) application. The client sends commands to the server which controls the front-end, reads data out and transfers results and data blocks back to the client. The client typically runs on a laptop and the server is embedded on the motherboard. The software repository can be accessed at the following link:

   `https://svnweb.cern.ch/trac/atlasgroups/browser/Detectors/TileCal/MobiDICK`

   And browsable via the command line in the address:

   `https://svn.cern.ch/reps/atlasgroups/Detectors/TileCal/MobiDICK/` .

5.1   Server

The server is a top level application that runs as a daemon on the motherboard. Part of the data analysis is performed on the server. It uses TCP sockets to communicate with the client and contains a set of functions to perform the different tests. It also has a library to access the hardware registers of different components in the system.

There is one class for each firmware device (core) that extends a base class. These classes allow easy read and write access to the different registers of each board. The server application can be compiled with gcc for test purposes, but has to be cross-compiled for PowerPC using Xilinx ISE ELDK13.1 in order to be executed on the motherboard. Finally it is stored in the system boot image along with the rest of the firmware for production.

A debug tool application called test-device allows direct access to any memory register on the motherboard. This tool is also deployed with MobiDICK.

To start the server, the user should use the telnet to connect to the Mobidick box and start the server.

5.2   Client

Willy is the user friendly client GUI for MobiDICK that uses TCP sockets to communicate with the sever. It presents itself as a window organized with tabs that describe the different tests. It is implemented in C++ using ROOT for the window manager and analysis framework. A few core packages define the main window and communication functionalities while the rest of the packages describe the tests as plug-ins to the main window which are loaded dynamically at run time.

Willy is released as a set of CMT packages organized in a cmt project. The Release package describes all the packages included in the project. Each single package explicitly enumerates the packages it depends on. The main window package is Willy.

To compile the packages, execute the following steps:

1. Download and compile the ROOT and CMT packages.

2. setup environment variables: source `CMTPATH/CMT/v1r26/mgr/setup.sh` and the ROOT system

3. Creating the "MobiDICK" directory.

470 4. make a directory "cmt" paralell with the "MobiDICK" and put "project.cmt" inside.
471   The "project.cmt" should have one line content "project mobidick".

472 5. In directory "MobiDICK", svn co `https://svn.cern.ch/reps/atlasgroups/Detectors/`
473   `TileCal/MobiDICK/Release ./`

474 6. python python `Release/trunk/scripts/init_release.py Release/trunk/cmt/`
475   `requirements`

476 7. make a directory "cmt" paralell with the "MobiDICK" and put "project.cmt" inside.
477   The "project.cmt" should have one line content "project mobidick".

478 8. setup environment variables: source `CMTPATH/CMT/v1r26/mgr/setup.sh` and the
479   ROOT system

480 9. Compile the packages: go to the MobiDICK/Willy/cmt, execute "cmt bro 'cmt
481   config' " and "cmt bro 'make'" and "cmt bro 'make inst'". The packages linked in
482   requirements will be compiled and installed automatically.

483 10. Copy the `MobiDICK/installed/machine-name/bin/Willy.exe` to Run/ and use
484   ./Willy.exe to start the programm. In the Run/ there are icons and parameter files
485   needed by the programme.

486 To add a new test, the user need prepare the parameter files, the test algorithms, the test
487 results and the GUI preference. All of these will be put into an individual package, which
488 is extended from the "TestFrame" and "TestParams". The new test will be compiled to
489 individual libraries and will be loaded in the run time. In Willy a request on performing a
490 particular test is sent to the server and the server transfers back the results by strings. So
491 the test algorithm should be implemented in the main.cpp in server as well. The sending
492 back results will be parsed and displayed in the GUI.
493   The packages of Willy are listed below:
494   Compilation of tagged Release versions of Willy is preferable as it ensure uniformity
495 and provides debuggers with a greater amount of information. Before updating to a new
496 release, make sure you know the Release tag you want to use, and replace it in line #4 (As
497 of 25/08/14 the current version is Release-14-08-25). You should also know the password
498 to the tilerod account, though in a pinch your own svn account will work. To updated to
499 a new tagged Release version from a computer that already has Willy, enter the following
500 commands into the terminal:

501 1. rm -rf /home/mobidick/Willy/MobiDICK/*

502 2. cd /home/mobidick/Willy/MobiDICK/

503 3. svn co svn+ssh://tilerod@svn.cern.ch/reps/atlasgroups/Detectors/TileCal/MobiDICK/Release/t
504   xx-xx-xx /home/mobidick/Willy/Mobidick/Release

505 4. python Release/scripts/init_release.py Release/cmt/requirements .

506 5. cd Willy/cmt/

Package name	Functionality
Environment:	
Policy	Policy for CMT compilation
RootInter	Root interface
ExpertCore	Expert system engine
Base functionalities:	
Servercomm	Communication via TCP/IP to the server
Kernel	Format of test results and superdrawer status
SDParams	Superdrawer parameters
TestFrame	Base class of test frames
TestParams	Base class of test parameters
Base GUI tools:	
FrameTools	Tools for widgets in the GUI
RootGuiTools	Tools for widgets in the GUI
SDGeometry3D	Superdrawer 3D view in the GUI
Individual tests:	
TestAdder	Test for the adder
TestCommHV	Test for the high voltage communication
TestCommMB	Test for the mother board communication
TestDigBase	Base class for digitizer test
TestDigCheck	Check the digitizer
TestDigNoise	Noise test
TestDigShape	Pulse shape test
TestInteg	Test for the integrator
TestNominalHV	Test for the high voltage
TestOpto	Test for the HV opto
TestStabilityHV	Stability test for HV
LedHVCtrl	LED HV control test
Willy	The main frame

Table 18: The package lists of Willy.

507 6. cmt bro 'cmt config'

508 7. cmt bro 'make && make inst'

Not reviewed, for internal circulation only

509 # 6   Front-end electronics tests

510 There are different tests required to certify each front-end electronics component. Failure
511 of a specific test indicates that the components being evaluated needs to be replaced. The
512 tests performed by the MobiDICK4 on the super-drawers are detailed in the following
513 paragraphs.
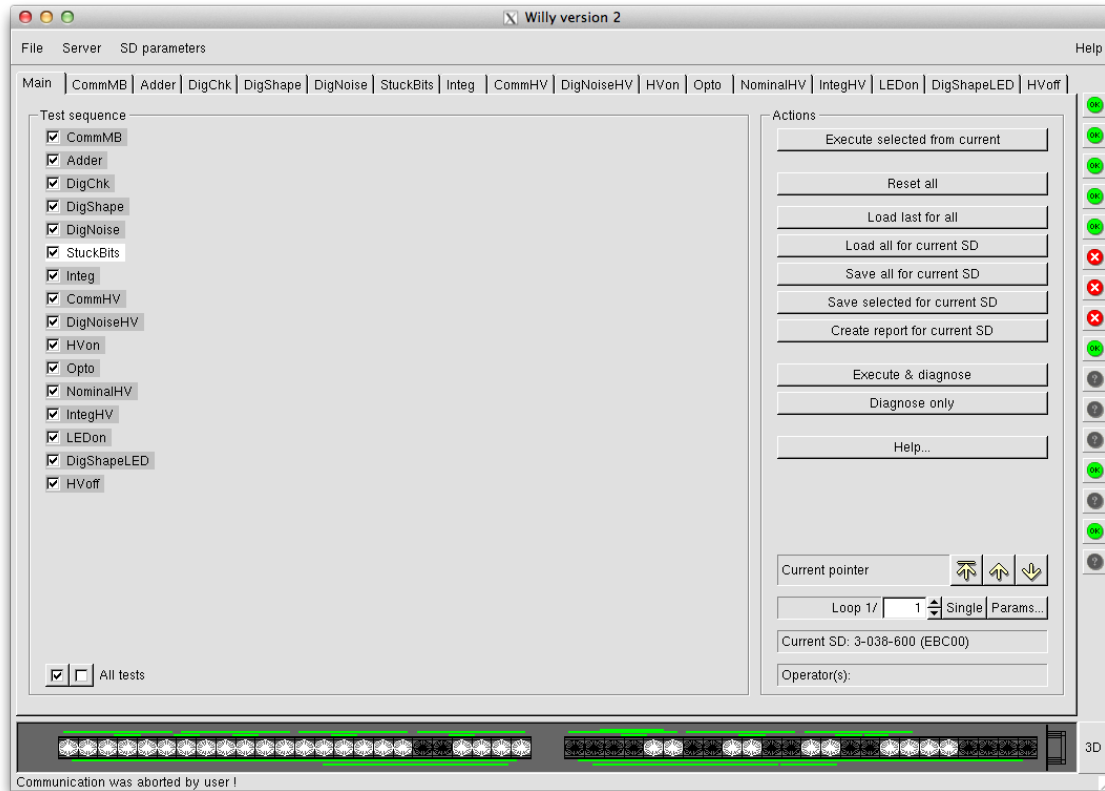
Figure 25: The main window of the Mobidick4 test

514 Each tab represents a different test. The tests can be loaded as plug-ins. They are
515 described in the following subsections.

6.1 Data integrity test (DigChk)

This is a test of the digital read-out. It comprises 5 sub-tests, four of which use the same digitizer mode (calibration) and different read-out mode from 0xA8 to 0xAB. The last sub-test is performed in the test mode of the digitizers (rolling bits) and read-out mode 0xA8.

For each sub-test, one single event is read-out and data quality is assessed by checking the CRC of each of the 16 DMUs along with the global event CRC one. The result of this test with one of the super-drawer of ATLAS is shown in Figure 26.
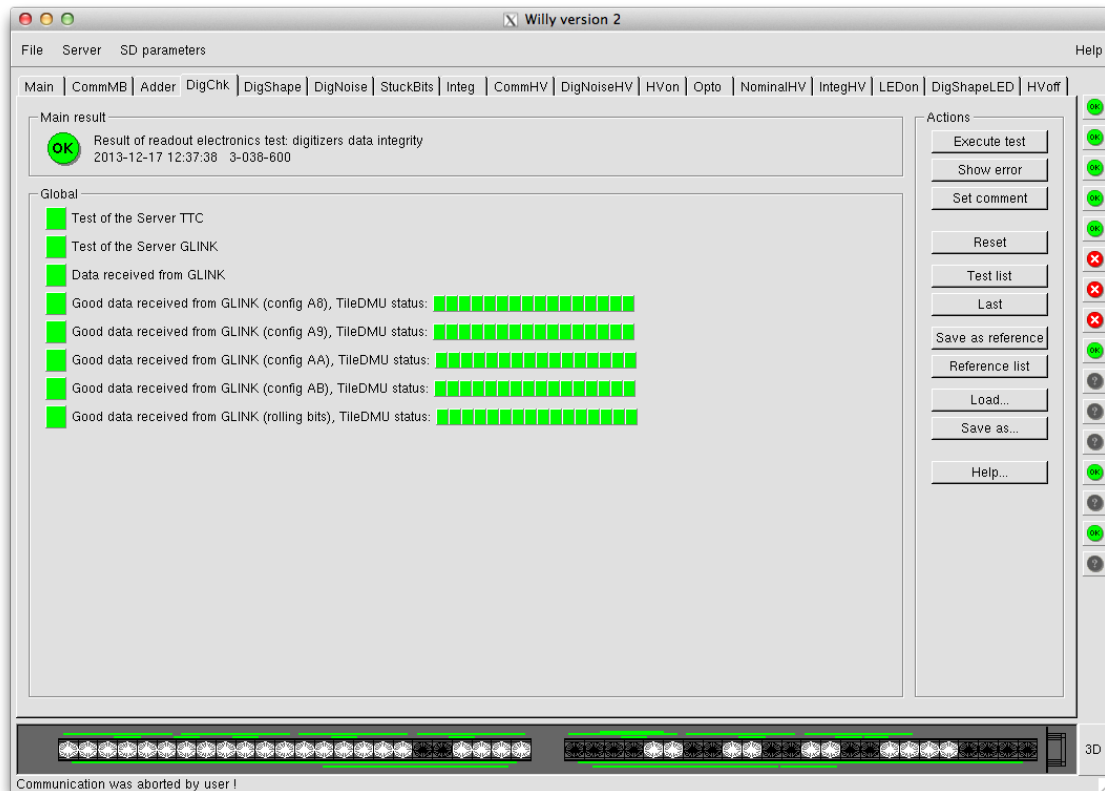
Figure 26: Example of a Data integrity test with a super-drawer in ATLAS

6.2   Communication with motherboard CAN (CommMB)

This is a test of the communication with the motherboard side of the drawer. The test runs through the following steps:

1. Establish communication with the ADC using CAN bus.

2. Read out the serial number of the ADC. The super-drawer associated with this serial number is searched for in the local or central databases.

3. The super-drawer parameters are compared to the central and local databases.

4. The firmware version of ADC is checked.

5. The 3-in-1 cards are configured with CAN bus and their configuration is read back with CAN bus.

6. The 3-in-1 cards are configured with TTC and their configuration are read back with CAN bus.

7. The TTCrx address of the mezzanine card is checked.

There is also the possibility of executing only the CAN bus part of the test. Figure 27 shows the result of the test with super-drawer.
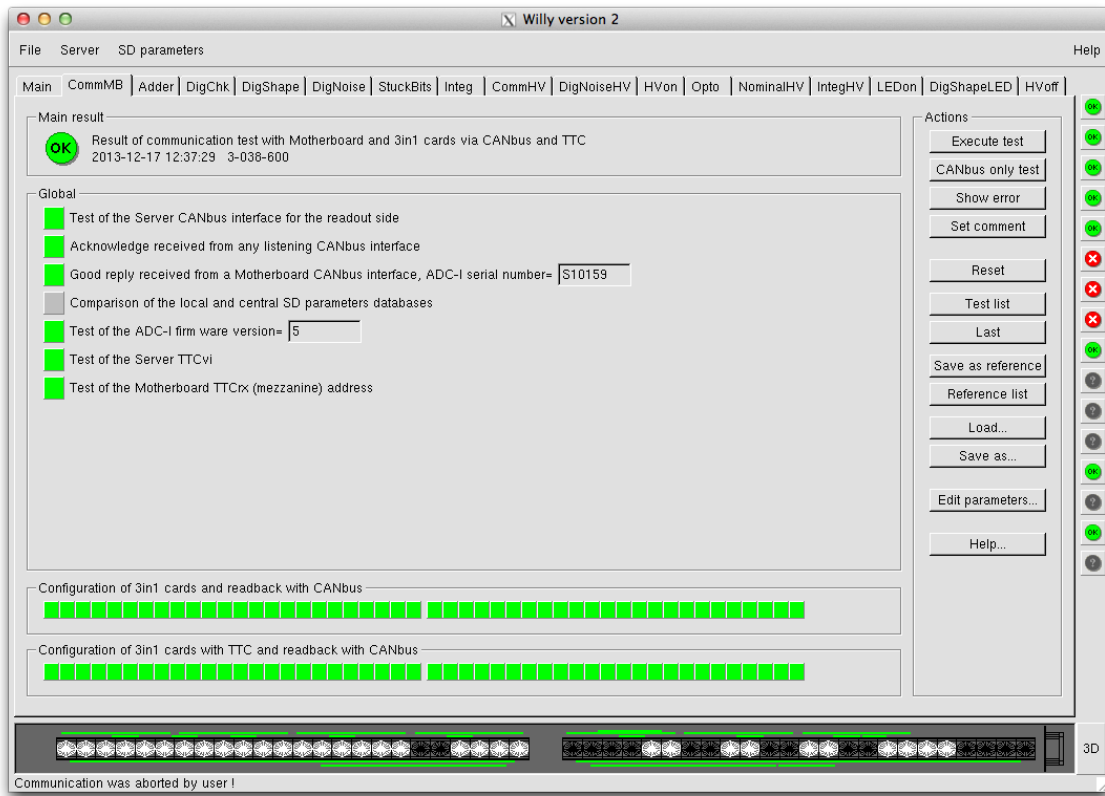
Figure 27: The result of communication with the motherboard CAN of a super-drawer in ATLAS.

6.3 Communication with HV CAN (CommHV)

This is a test of the communication with the High Voltage side of the drawer and a check of its status. The steps are:

1. The communication with HVmicro using CAN bus is established.

2. The software version of HVmicro is checked.

3. The global status register of HVmicro is checked.

4. The input low voltages are checked.

5. The temperature probes are checked.

6. The serial numbers of the HVmicro and the two HVopto cards are checked.

Figure 28 is the test result with the super-drawer in ATLAS.
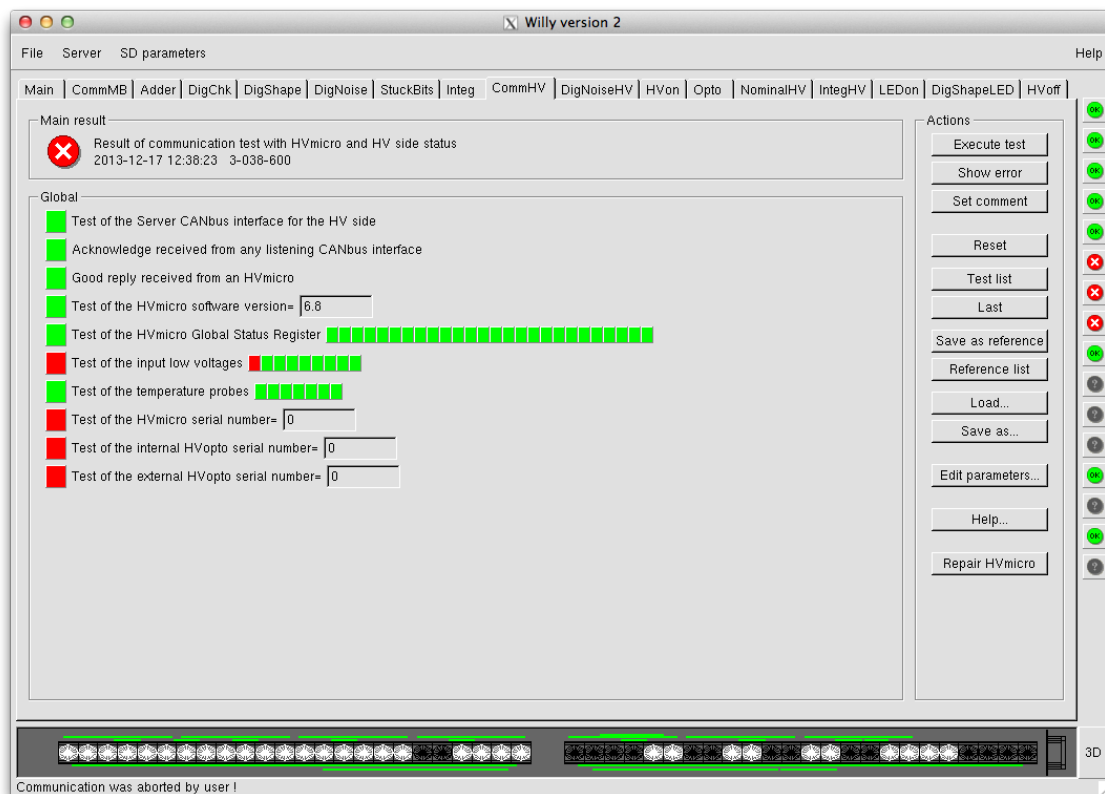
Figure 28: The result of Communication with HV CAN with a super-drawer in ATLAS

6.4   Trigger tower charge injection test (Adder)

This test checks the response of the adder summation card (adder) to a known injected charge. The test first goes through an initialization during which the folllowing are done:

1. Test and configure the Server TTC for the selected module. Charge injection is removed.

2. Initialize and configure the ADC trigger board. The signal coming out of the trigger cables are digitized using the trigger ADC set of cards in MobiDICK. There is only one pedestal value for each adder card.

The "Execute test" button tests the trigger ADC readout for each of the channels in the module seccessively. In each channel a configurable amount of change is injected, and the trigger signals are read out from Hadron and Muon adders separately with different gains. After the test is finished, each channel box is given a color indicating the test status:

1. Grey means the channel is not tested.

2. Green means a good 3-in-1 card.

3. Blue means the channel belongs to no Hadron or Muon adder (a good hole).

4. Cyan means the channel is very noisy (large RMS for the pedestal).

5. Red means all other kinds of problems.

Detailed information about the channel test result can be retrieved by clicking on the channel box symbol you are interested in. Two plots will be shown for this channel in the bottom left panel:

1. The left plot shows the trigger (Hadron or Muon) signal as a function of the sample number from the trigger adder that this channel belongs to. The error bars indicate the RMS of the pedestal region. The green dashed line indicates the pedestal level.

2. The right plot shows the trigger (Hadron or Muon) signal, with the pedestal subtracted, coming from different adders in response to the charge injection in this channel. The first 9 (last 7) bins are for the Hadron (Muons) adders. The Hadron (Muon) adder that this channel belongs to is indicated by a green (blue) color. The bin will be empty if no adder is implemented. A green (blue) dashed line indicates the Hadron (Muon) signal threshold below which the signal is considered to be not good. It is expected that only the adder containing the channel will give a trigger signal above the threshold line, while the remaining adders will give zero signals below the thresholds. This plot is also useful to check the correlations of the trigger signals coming out from different adders in the selected module.

⁵⁸⁴ The text box to the right of the plot panel shows some detailed information about ⁵⁸⁵ this selected channel, such as the signal and pedestal values, the error explanations, etc. ⁵⁸⁶ There are also 4 clickable boxes at the bottom right corner, by clicking on which a few ⁵⁸⁷ summary plots will be shown:

⁵⁸⁸ 1. The trigger signal (with pedestal subtracted) and pedestal distributions of all the ⁵⁸⁹   channels in the module.

⁵⁹⁰ 2. The trigger signal (with pedestal subtracted) as a function of the channel number.

⁵⁹¹ 3. The trigger pedestal RMS as a function of the channel number.

⁵⁹² The user should define a signal window with sample numbers for the left and right ⁵⁹³ edges. The pedestal is calculated outside of the signal window (pedestal region), and the ⁵⁹⁴ signal is the integration of the ADC counts inside the signal window, with the pedestals in ⁵⁹⁵ each bin subtracted. The following parameters can be configured by the user by clicking ⁵⁹⁶ on the "Edit parameters" button:

⁵⁹⁷ 1. The number of events and samples.

⁵⁹⁸ 2. Hadron and Muon signal thresholds (below which means not good).

⁵⁹⁹ 3. Hadron and Muon pedestal RMS thresholds (above which means noiny).

⁶⁰⁰ 4. Signal window low and high edge (sample number).

⁶⁰¹ 5. Hadron and Muon signal conversion factors. These factors are applied to all the trig- ⁶⁰²   ger ADC readouts, either to convert the ADC counts to pC, or to make the Hadron ⁶⁰³   and Muon readouts commensurate in the same plot. Note that the thresholds are ⁶⁰⁴   not scaled by the conversion factors.

⁶⁰⁵ The "Single test" performs similar tasks as the "Execute test", except that the test ⁶⁰⁶ is done on a single selected channel. After the tests, the test results can be save into a ⁶⁰⁷ text file by clicking on the "Save as" button. The results from previous tests can also be ⁶⁰⁸ loaded in and visualized by clicking on "Last" or "Load". Figure 29 shows an example ⁶⁰⁹ test result with a selected super-drawer.

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Figure 29: Example of a trigger tower charge injection test with a selected super-drawer, with 100 samples and 1 event for each channel.

6.5 Digitizer charge injection test (DigShape)

The purpose of this test is to check the digitizer functionality and the data readout. Using the charge injection circuit[12, 13], the two amplification circuits of the digital readout can be obtained via the Charge Injection System (CIS). The test goes though following steps:

1. At the beginning of the test, the digitizers are configured in auto-gain and readout mode 0xAB.

2. Two events are triggered: one for a small charge that will read out the high gain samples, and another one with a big charge that will read out the low gain samples.

3. Each event is analysed separately and is compared to the expected pulse (height and width) for the given charge.

This test also detects a missing connection between the 3-in-1 and the digitizer channel. For this test the execution of functions does not follow a sub-test structure. DIGI is executed in the first place followed by two calls to DIGA. The result of the test with an ATLAS super-drawer is shown in Figure 30.
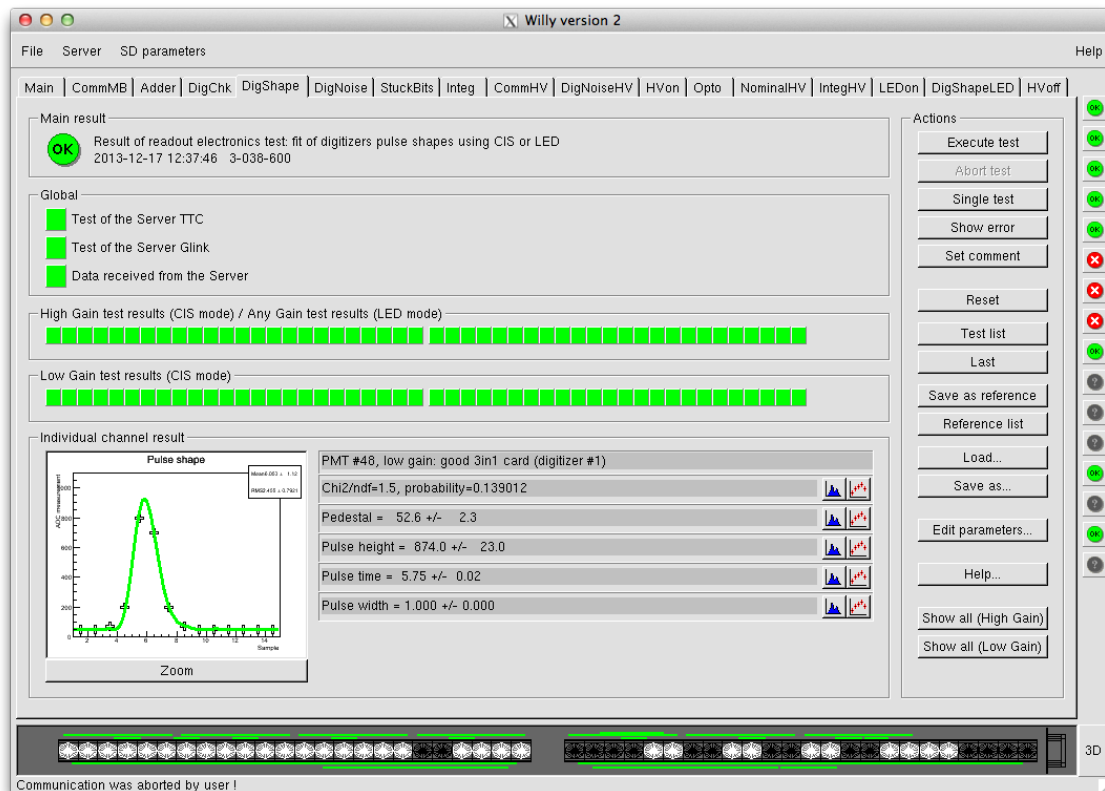
Figure 30: Example of a digitizer charge injection test with the super-drawer in ATLAS

6.6   LED test (DigShapeLED)

This test checks the response of the PMT to a light pulse emitted from an LED source similar to the one produced by particles in the tiles. It uses the b-channel FIFO to synchronize an LED pulse command that is interpreted by the HV+LED ip-core and triggers the LED driver and a L1A. The measured propagation time through the LED driver is 2 BC. This means that the L1A is sent to the pipeline with a 2 BC delay with respect to the LED pulse. The digitizers' data is read out and analysed by including a fit of the digitized pulse shape shown in Figure 32 and Figure 33.
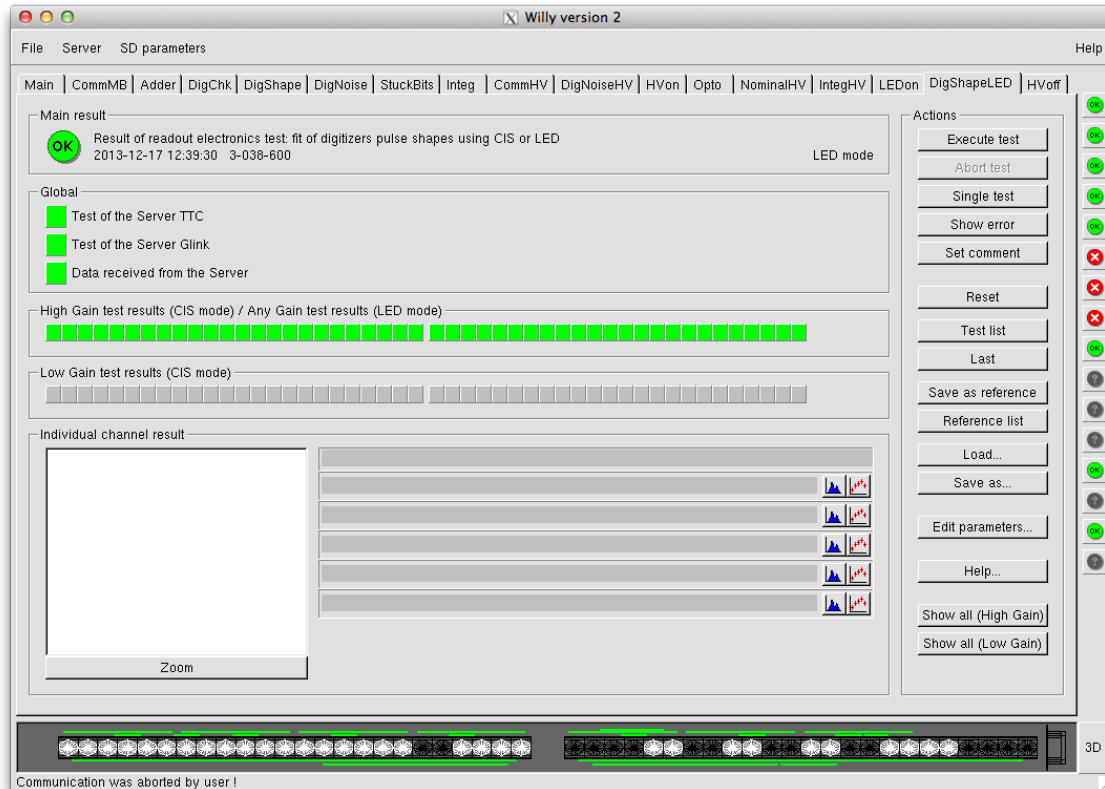
Figure 31: The responses of the super-drawer in ATLAS in DigShapeLED test

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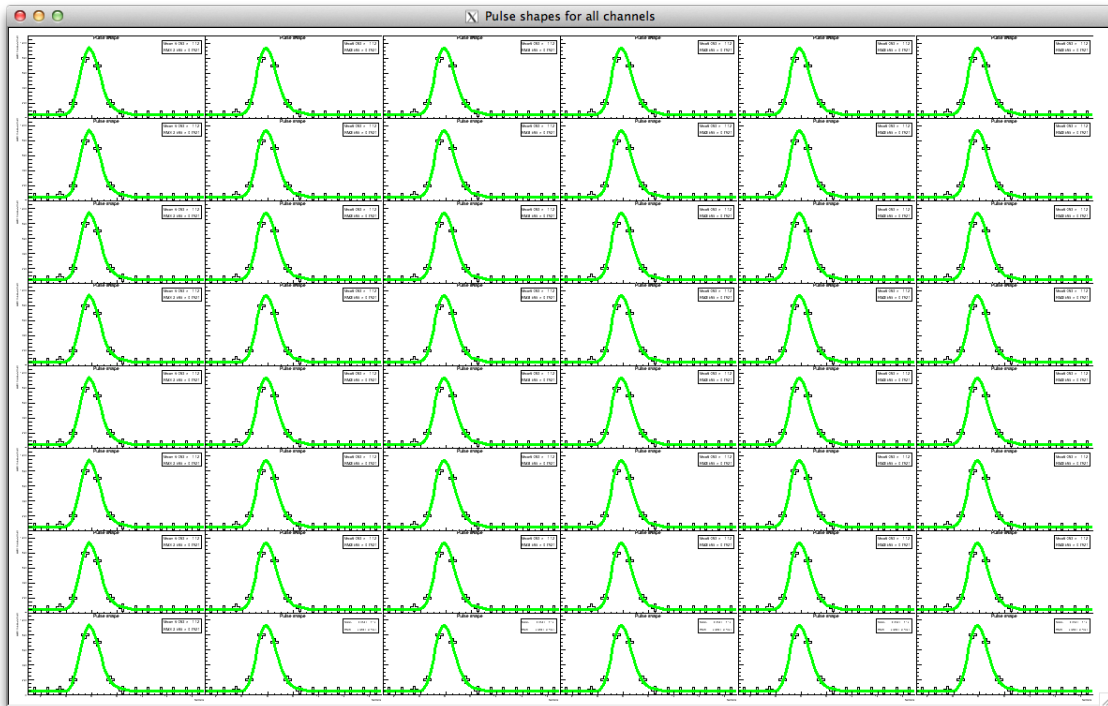
Figure 32: The responses of the super-drawer in ATLAS in DigShapeLED test at the high gain
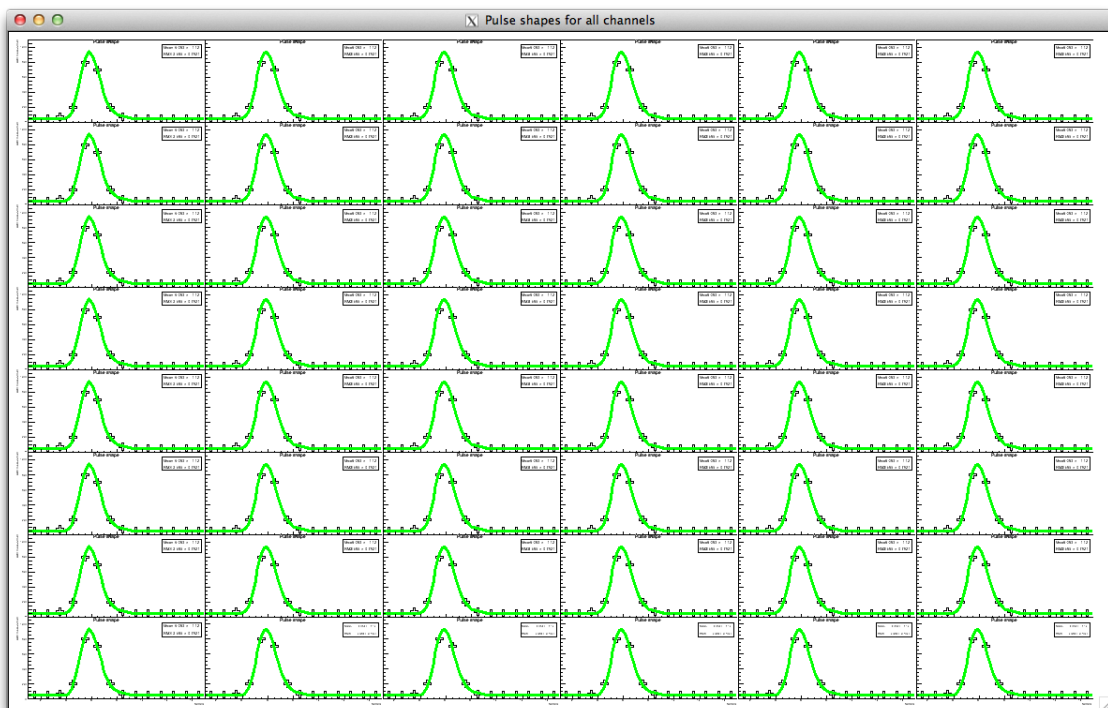
Figure 33: The responses of the super-drawer in ATLAS in DigShapeLED test at the low gain

6.7   Noise test (DigNoise)

The purpose of this test is to measure the digitizer noise and to check the data integrity. One thousand events are read out at maximum trigger rate to have reasonable statistics and the results only contain the pedestal information. The digitizers are in calibration mode in order to read both high gain and low gain data :

1. The BCID's of all TileDMUs are checked.

2. All CRCs are checked.

3. The pedestal average and RMS for each channel are computed and checked.

The test is performed with the high voltage distribution electronics off and a digitizer configuration of 0xAB for the event and bunch counter. DIGI is followed by a DIGP. Figure 34 shows one of the responses with the super-drawer in ATLAS.
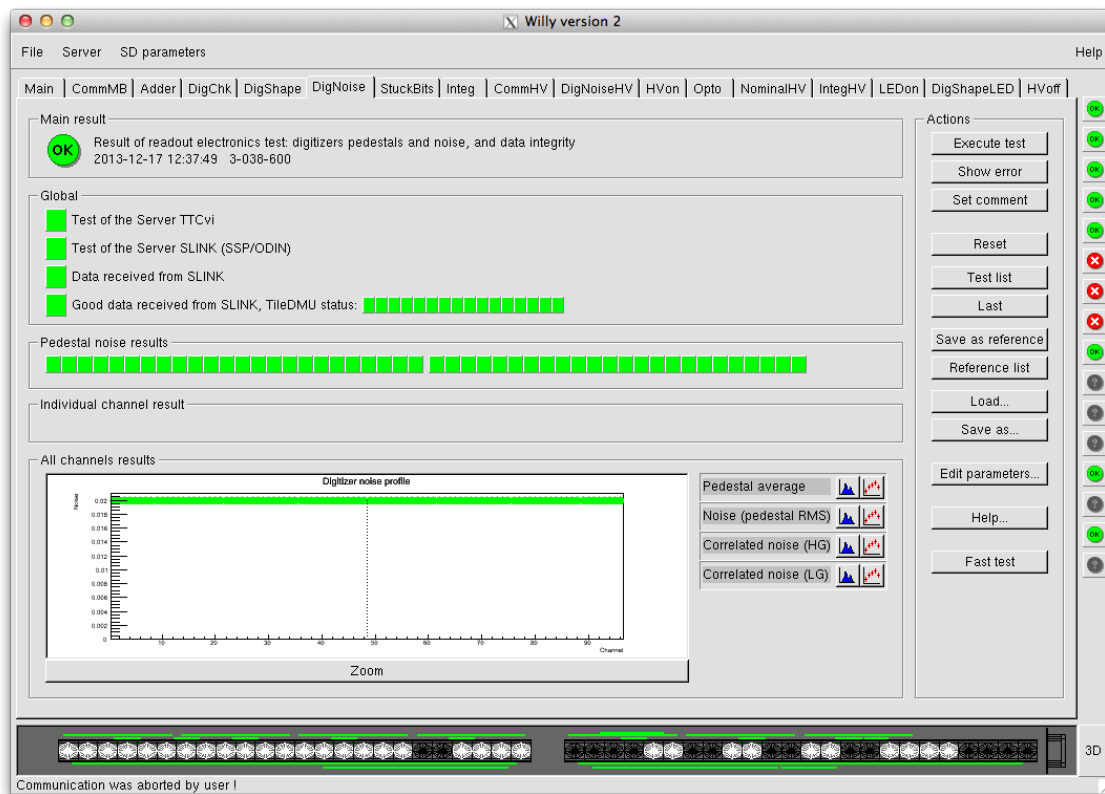
Figure 34: The responses of the super-drawer in ATLAS in DigNoise test

6.8   Noise test with HV (DigNoiseHV)

Using the same setup as DigNoise but with the high voltage distribution electronics on to measure the noise level. However, no HV is provided to the PMTs. The same profile showing the noise evolution with respect to the channel number can be repeated to check the HV's effect on the digitizer noise. Figure 35 is a sample response of the super-drawer in ATLAS while the DigNoiseHV test is running.
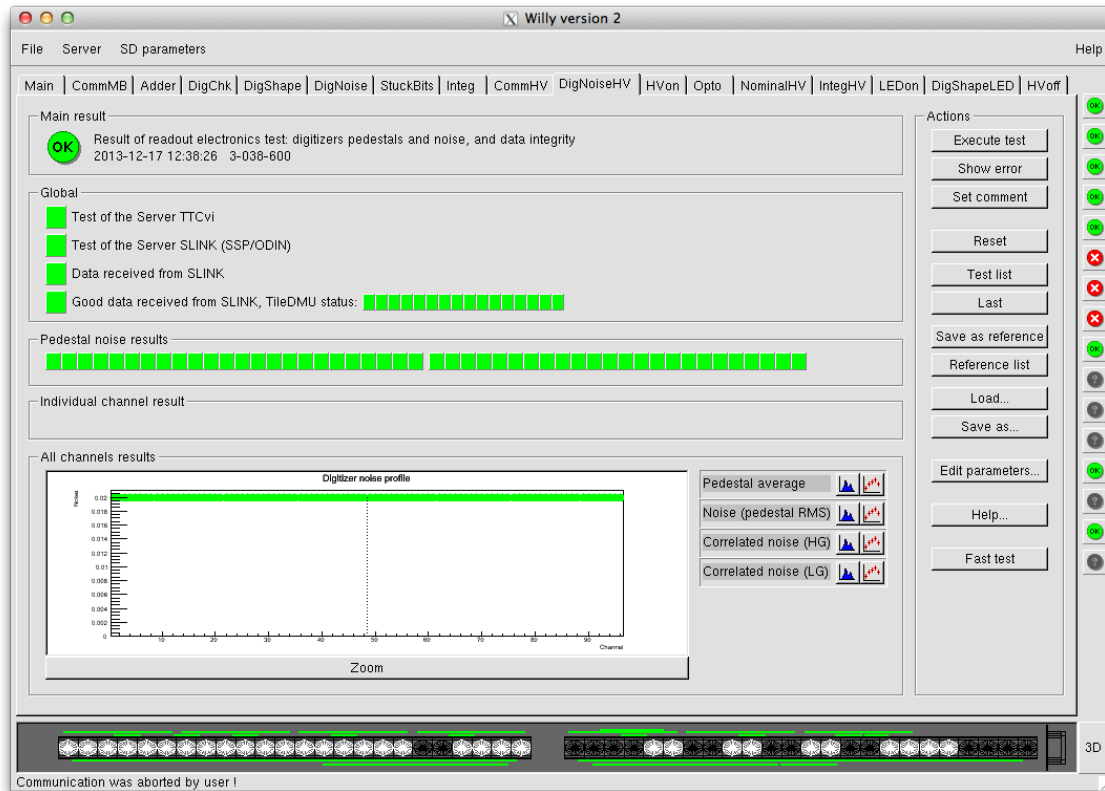
Figure 35: The responses of the super-drawer in ATLAS in DigNoiseHV test

6.9   Stuck bits test (StuckBits)

This test is implemented to detect upset bits in the samples caused by failures in the front-end-digitizer boards by flipping all the bits of the 10-bits digitizer read-out many times. Any bit that does not flip in state is marked as potentially stuck. This is accomplished by injecting three different charges at three different injection times and using two different pedestal levels. The procedure is outline below.

1. Charge is set to a given value and several events are taken

2. Time is set to a value and several events are recorded

3. Pedestal is set to a value

4. Procedure is repeated many times to determine if there is a stuck bit
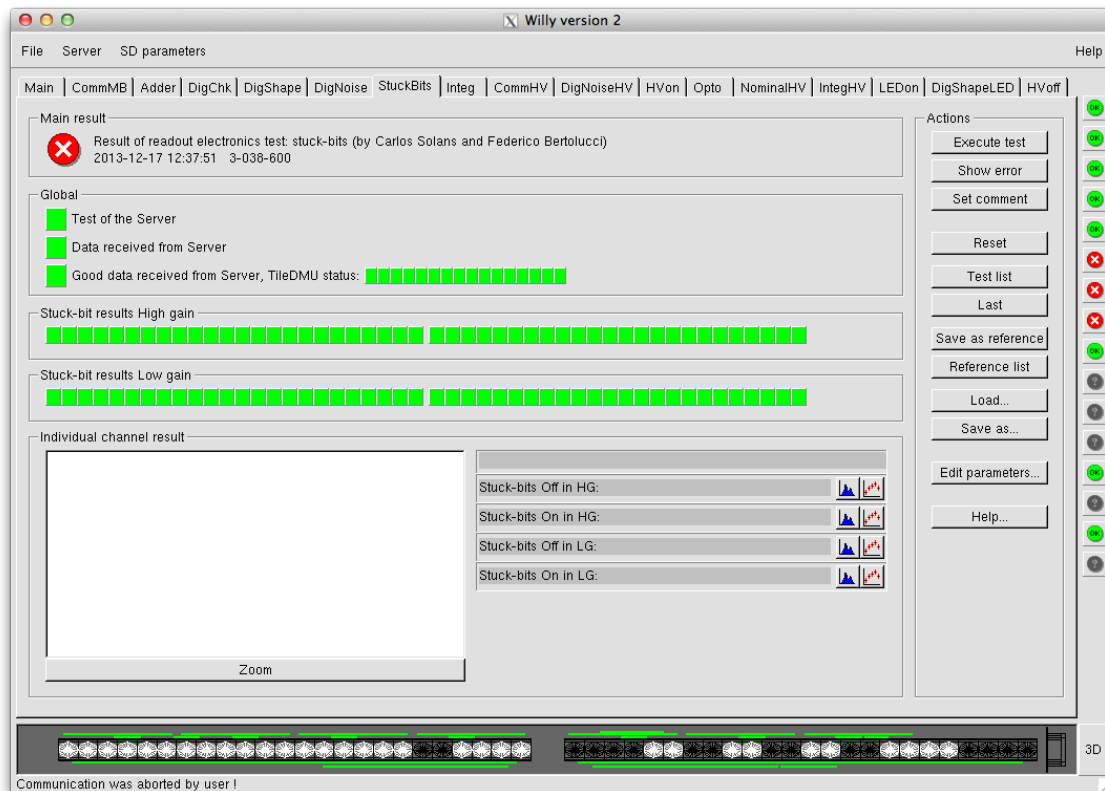

Figure 36: The responses of the super-drawer in ATLAS in StuckBits test

6.10   Integrator read-out test (Integ)

The purpose of these tests is to check the linearity and noise level of the ADC-I and of the charge integrator circuits of the 3in1 cards. This is done as follows:

1. For each single 3in1 card and for each charge integrator circuit gain, the pedestal RMS is computed over one hundred measurements and verified.

2. The charge integrator input is connected to DAC, with increasing settings. Its output is digitized by the ADC-I and checked to vary linearly. The slope is also verified.

The result of the test is shown in Figure 37.

Figure 37: Example of the Integ read-out test with super-drawer in ATLAS

6.11   Integrator readout test with HV (IntegHV)

This test checks only the pedestal RMS but with the high voltage distribution electronics and the high voltage input on. The same steps used in the Integ test are repeated for the IntegHV test to measure the linearity between the digitized injected charge (DAC) and the digitized response (ADC) that is obtained after the ADC-Integrator(ADC-I) card. The result of the test is shown in Figure 38.
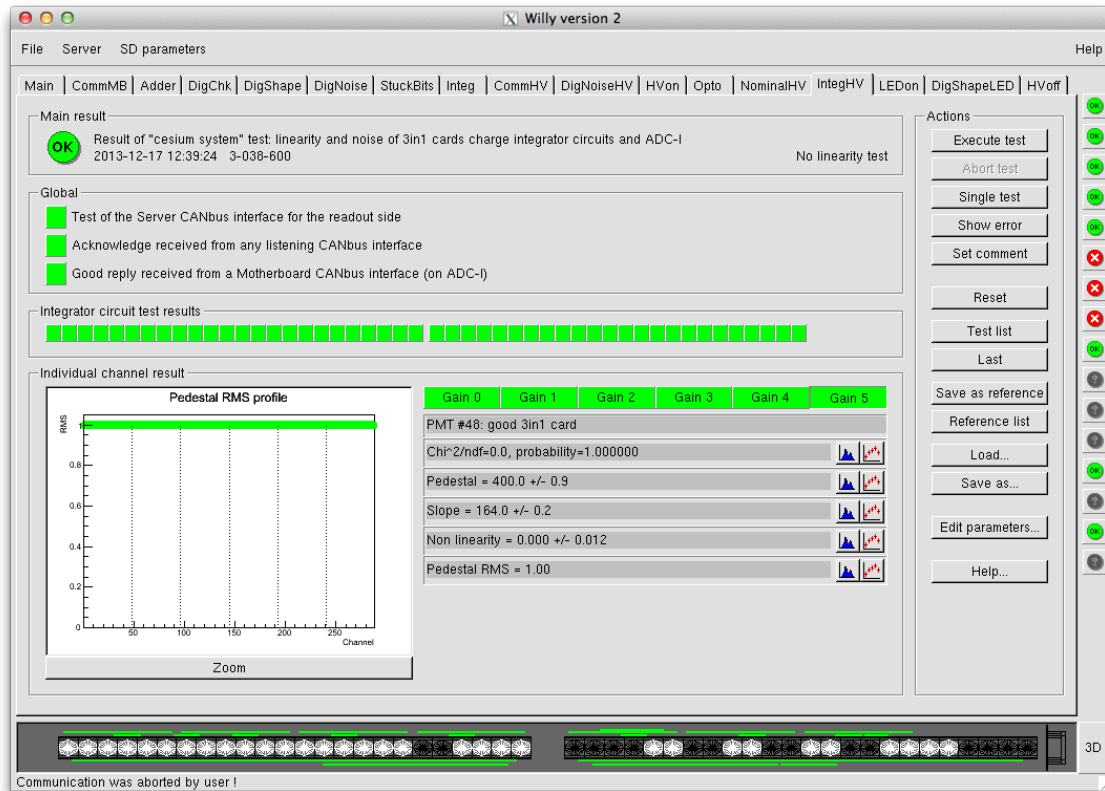
Figure 38: Example of the Integ readout test with HV test with super-drawer in ATLAS

675 ## 6.12   HV on

676 High voltage is turned on by the HV driver upon command HV_ON to HV+LED ip-core.
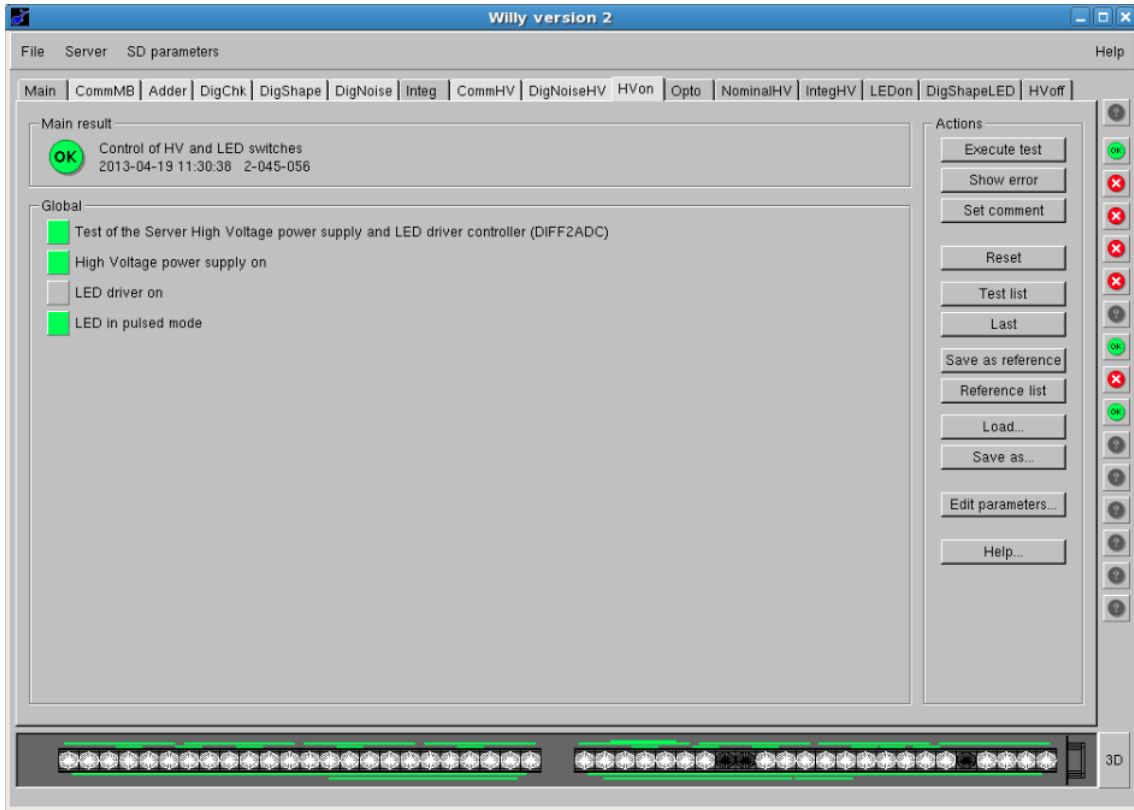The LED light starts flashing.

Figure 39: HV ON test

677

678 ## 6.13   HV off

679 High voltage is turned off by the HV driver upon command HV_OFF to HV+LED ip-core.
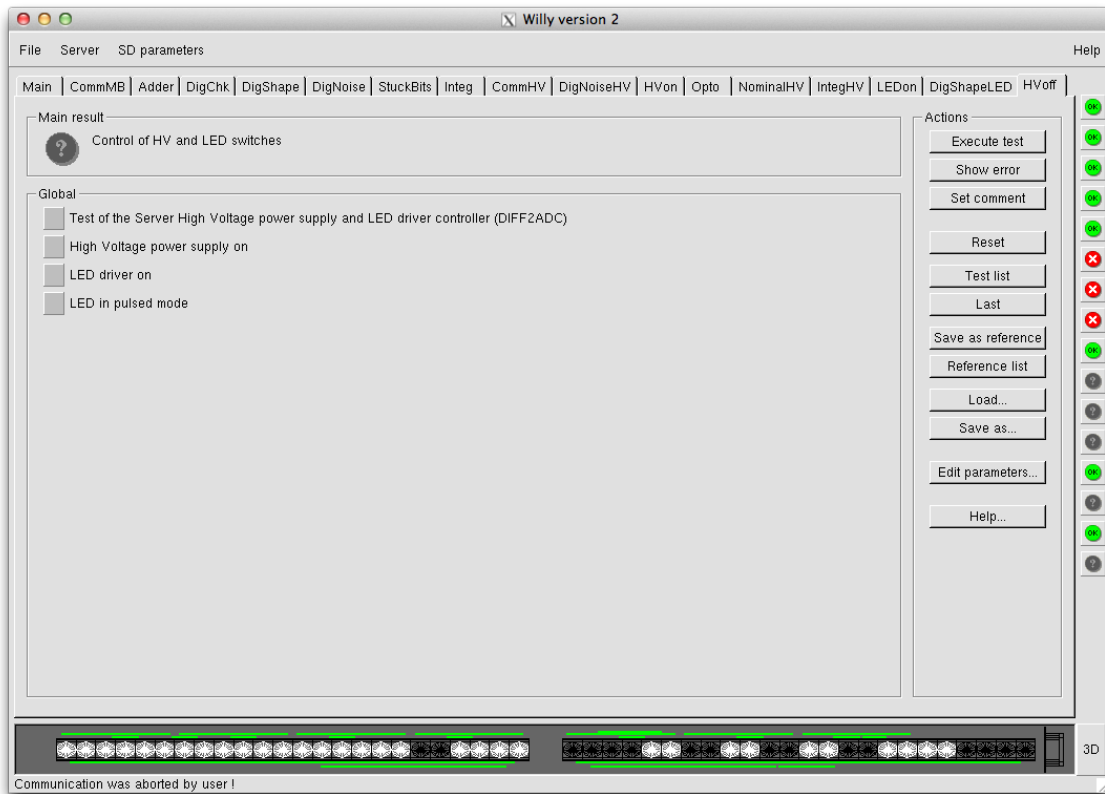680 The LED light stops flashing.

Figure 40: HV OFF test

6.14   HV distribution test (Opto)

The purpose of these tests is to check the functionality of the high voltage distribution electronics. For the Opto test:

- The four HV switches (odd/even internal/external) are all switched off. Then they are switched on one by one and verified;

- The HV is set to 700 V on all the channels. Then, for each channel, the measured voltage is read out and compared to the expected one.

- The HV is set to 600 V on all the channels. Again, for each channel, the measured voltage is compared to the expected one.
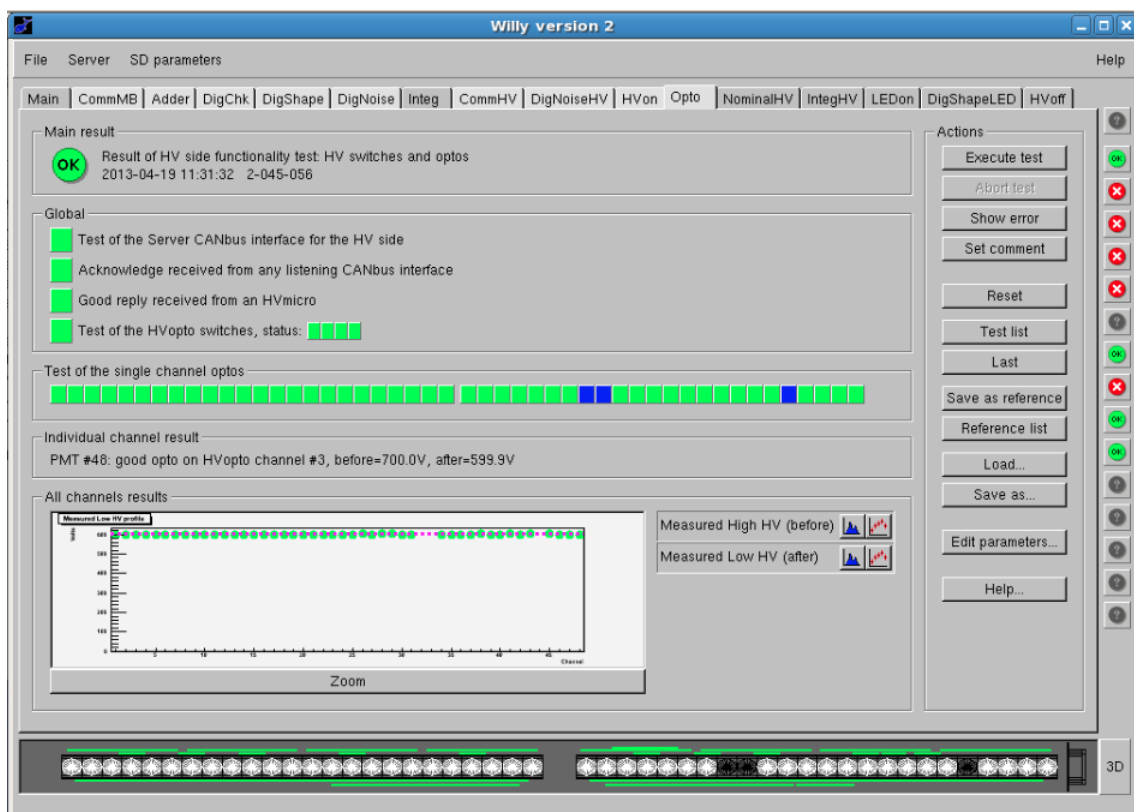

Figure 41: Example of HV distribution test

6.15 HV regulation test (NominalHV)

This test is similar to the Opto test but the voltage value set is the one stored in the HVMicro's EEPROM. The value is read back and compared against the super-drawer database.

Figure 42: Example of the HV regulation test

6.16 Turn on LED (LEDon)

The pulse mode of the LED driver is enabled. The purpose of this test is to check that the LED driver board is emitting pulses with -20 V amplitude and a width of 100 ns at a frequency of 1 kHz.
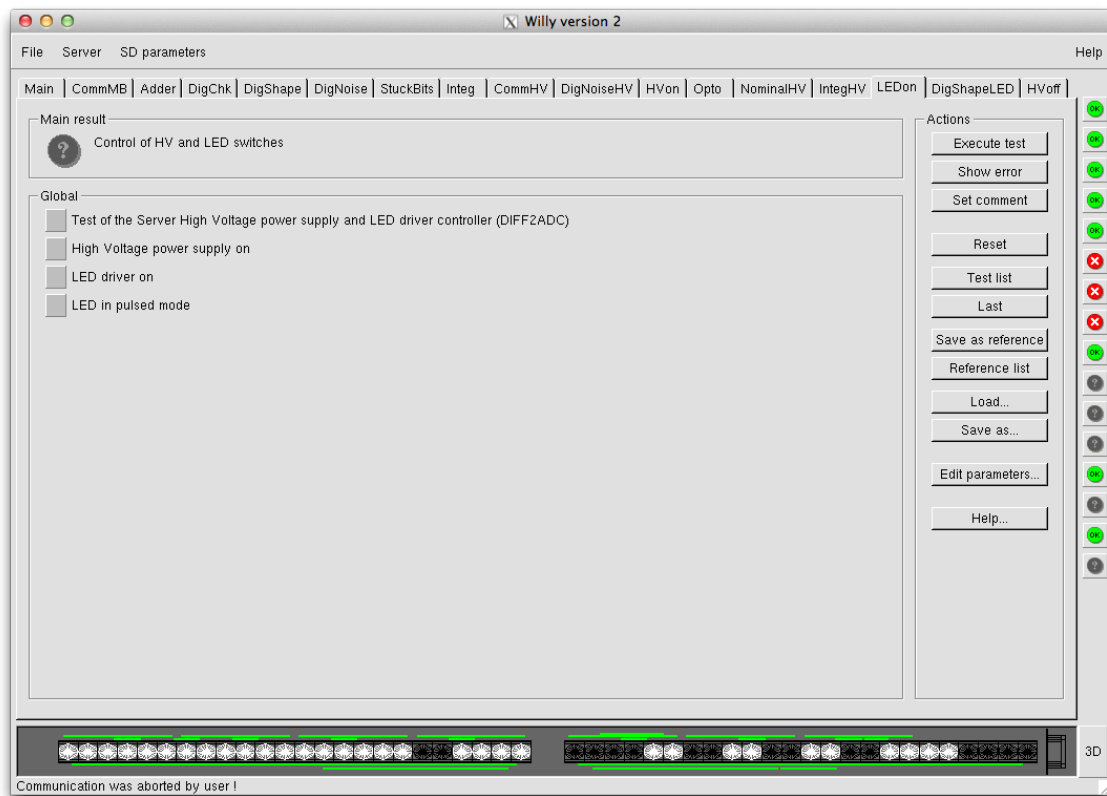
Figure 43: LED on test

7   Conclusions

MobiDICK is the in-situ certification tool of the TileCal front-end electronics in the AT-LAS experiment used in the commissioning phase and maintenance campaigns of the detector. A new version of this test-bench, MobiDICK4, has been conceived in order to guarantee its availability for future maintenance campaigns. This new implementation ensures an extended lifetime for the test-bench by replacing the obsolete technology with commercial components and custom built mezzanines. A detailed description of each of the boards is provided and important parts of the schematics are highlighted. This will allow the evaluation of the current design for future upgrades of the system. Characterization and performance measurements of the newly designed hardware components are outstanding.

The new test-bench is lighter to carry and faster to operate, and has been designed according to the requirements of the maintenance team whenever possible. Four tests have been improved and one has been added in order to increase the reliability of the certification procedure that takes place in the detector area to match similar procedures that are performed offline. A detailed description of the software is given allowing for incorporation of new tests.

Overall, the modular design of MobiDICK4 has been respected, allowing it to be easily adapted to the needs of a test-bench for a particular component of the front-end electronics. MobiDICK remains an autonomous DAQ system, capable of providing configuration and read-out interfaces to the TileCal front-end super-drawers.

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